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A 5.8-GHz Wideband TSPC Divide-by-16/17 Dual Modulus Prescaler

Wenrui Zhu, Haigang Yang, Tongqiang Gao, Fei Liu, Tao Yin, Dandan Zhang, and Hongfeng Zhang

***Abstract*— A high-speed CMOS TSPC divide-by-16/17 dual modulus prescaler is proposed. The speed of the prescaler is improved in two aspects. First, by adopting a new pseudo divide-by-2/3 prescaler, the minimum working period is effectively reduced by half a NOR gate's delay. Second, by changing the connection of TSPC D-Flip-Flops, the minimum working period is further reduced by half an inverter's delay. Simulation results show that the maximum operating frequency of the proposed circuit is improved by ∼40% compared with conventional circuit. Fabricated in 0.18-μm CMOS process, the proposed circuit is capable of operating up to 5.8 GHz. The power consumption is 2.6 mW at the maximum operating frequency under 1.6 V supply voltage.**

***Index Terms*— Dual-modulus prescaler, high speed, pseudo divide-by-2/3 prescaler, TSPC.**

I. Introduction

Dual-modulus frequency prescaler plays an important role in phase-locked loop (PLL) designs [1]–[5]. Although current-mode logic and inject locking prescaler can provide working frequency of hundreds/tens GHz with process of SoI CMOS or InP DHBTs and so on, TSPC dual-modulus prescaler is widely utilized in several GHz with standard CMOS process [4], [5]. It has the merits of single clock phase, low power, small area, and large output swing. Improving the speed is an important design issue for TSPC prescaler. In addition, several techniques have been developed. In the transistor level, forward body biasing technique can improve the speed by decreasing the threshold voltage of nMOS transistors [6], [7]. However, it suffers from high minimum working frequency as well as increased cost and decreased robustness. In the gate level, adopting extended-TSPC flip-flops can effectively improve the operating speed [5]. But the current leakage is serious, thus the minimum working frequency performance is limited. In the RTL level, improving the speed of divide-by-2/3 prescaler can also enhance the speed of divide-by-16/17 prescaler [8], [9]. However, in these papers, several design rules of TSPC circuits are broken. It leads to shrinking frequency range because these prescalers are no longer suitable for low frequency operation.

Now both the divide-by-4/5 and divide-by-2/3 prescaler are widely utilized [4], [5]. Usually, divide-by-2/3 prescaler has the speed advantage and is much more power efficient. Thus, divide-by-2/3 prescaler is preferred in 16/17 prescalers. On the other hand, in the application background with a large division ratio, such as 128/129 prescalers, divide-by-4/5 helps to reduce the critical path and is more preferred.

In this brief, the maximum working frequency of the divide-by-16/17 prescaler is improved in two aspects. First, a novel pseudo divide-by-2/3 prescaler is developed and adopted into the divide-by-16/17 prescaler. It leads the minimum working period to reduce by half a NOR gate's delay. Second, by changing the connection of TSPC D-flip-flops (DFFs), the minimum working period is further reduced by half an inverter's delay. Fabricated in 0.18-μm CMOS technology, the circuit achieves a maximum working frequency of 5.8 GHz. The measured working frequency range is from 2 MHz to 5.8 GHz.

This brief is organized as follows. Sections II and III introduce the conventional and proposed divide-by-16/17 dual modulus prescaler, respectively. The measurement results are presented in Section IV and the conclusion is given in Section V.

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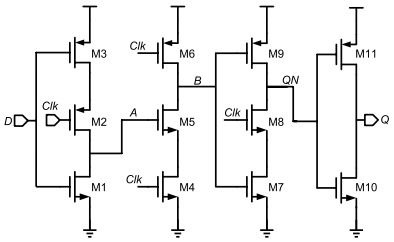

Fig. 1. Structure of TSPC DFF.

II. Conventional Divide-by-16/17 Dual-Modulus Prescaler

A. TSPC D-Flip-Flop

Fig. 1 shows a popular structure of TSPC DFF [10], [11]. The setup time of the TSPC DFF can be written as

$$t_{\text{setup}} = t_{D\_A} \tag{1}$$

where t_{D_A} means the propagation time from node D to node A, which is a clocked inverter's delay. The propagation delay of the TSPC DFF can be written as

$$\begin{aligned} t_{d\_QN} &= t_{A\_B} + t_{B\_\text{QN}} \\ t_{d\_Q} &= t_{A\_B} + t_{B\_\text{QN}} + t_{\text{QN}\_Q} \end{aligned} \tag{2}$$

where t_{d_QN} and t_{d_Q} are the propagation delay from CLK to QN and Q, respectively. t_{A_B}, t_{B_QN}, t_{QN_Q}represents the propagation delay from node A to B, B to QN, and QN to Q, respectively.

An advantage of TSPC circuits is that AND/OR logic gates can be absorbed into the first stage of TSPC DFFs and the logic depth can be reduced [10]. After AND/OR gate absorption, the first stage of the TSPC DFFs will become a clocked NAND/NOR gate. The logic depth can be reduced by about two inverters' delay after absorption. Usually, there are various structures to realize the required function by utilizing logic gates and TSPC DFFs. The optimized design is to employ only one AND/OR logic gate before one TSPC DFF. Then, the TSPC DFFs absorb all the logic gates into their first stages. After this, the logic depth, power consumption, and layout area will all be reduced.

Above all, the design rules of TSPC circuits should be followed. First, it will be better if the logic should be embedded in the first stage of TSPC DFF, but not other stages. Second, it is not suggested that two path controls one node. Otherwise, conflictions and glitches may happen.

B. Conventional Divide-by-16/17 Prescaler

Fig. 2 shows the schematic of a conventional divide-by-16/17 prescaler based on a divide-by-2/3 prescaler [8]. It has two critical

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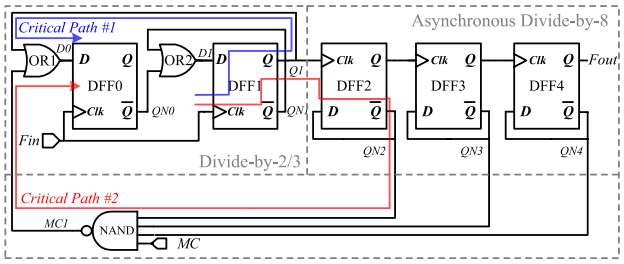

Fig. 2. Schematic of conventional divide-by-16/17 prescaler.

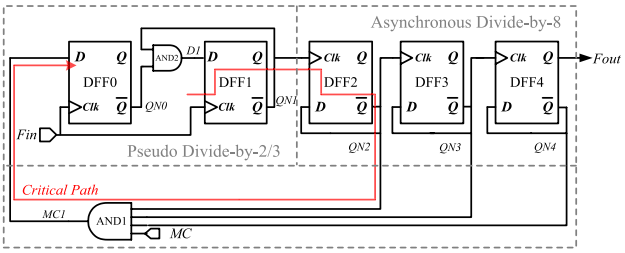

Fig. 3. Schematic of proposed divide-by-16/17 prescaler.

paths: 1) Q1 path (critical path #1) comes through DFF1 and OR1 and 2) MC1 path (critical path #2) comes through DFF1, DFF2, NAND, and OR1. Signal must pass path #1 within a period of Fin while it should pass path #2 within two periods of Fin.

Since OR1 and OR2 can be absorbed into the TSPC DFFs, the minimum working period $T_{\text{min,con}}$ of Fig. 2 can be written as

$$T_{\text{min,con}} = \max \left\{ \begin{array}{l} t_{d\_Q,\text{DFF1}} + t'_{\text{setup,DFF0}} \\ \dfrac{t_{d\_Q,\text{DFF1}} + t_{d\_\text{QN,DFF2}} + t_{d,\text{NAND}} + t'_{\text{setup,DFF0}}}{2} \end{array} \right\} \quad (3)$$

where $t_{d\_Q,\text{DFF1}}$ represents the propagation delay from CLK to Q1 of DFF1, $t_{d\_\text{QN,DFF2}}$ represents the propagation delay from CLK to QN2 of DFF2, $t'_{\text{setup,DFF0}}$ is the setup time of DFF0 with absorbed OR1, and $t_{d,\text{NAND}}$ is the NAND gate delay.

In theory, it is difficult to estimate which path decides the minimum working period. The result varies in different designs. It is a tradeoff between lengths of the two critical paths in conventional divider-by-16/17 prescaler. The optimized design is to make the length of critical path #1 approximately equal to half length of critical path #2. Then, the first term and second term in the right hand of (3) will be equal. Equation (3) can be rewritten as

$$T_{\text{min,con}} = \frac{t_{d\_Q,\text{DFF1}} + t_{d\_\text{QN,DFF2}} + t_{d,\text{NAND}} + t'_{\text{setup,DFF0}}}{2}. \quad (4)$$

In conventional divide-by-16/17 prescaler, two logic gates (NAND and OR1) locate in front of DFF0. Apparently, it is not the optimized design. In addition, there are two critical paths. Both critical paths should be optimized to achieve a high speed, which is a great challenge for designers.

III. Proposed Divide-by-16/17 Prescaler

Fig. 3 shows the schematic of the proposed divide-by-16/17 prescaler. It consists of a pseudo divide-by-2/3 prescaler, an asynchronous divide-by-8 divider, and a four-input AND gate. Compared with the conventional circuit, there are two main changes in the proposed divide-by-16/17 prescaler. First, a new pseudo divide-by-2/3 prescaler is adopted instead of conventional divide-by-2/3 prescaler. The pseudo divide-by-2/3 prescaler can exactly accomplish a single, but not continuous divide-by-3 operation. In addition, it is enough for divide-by-16/17 prescaler because it only needs less than one

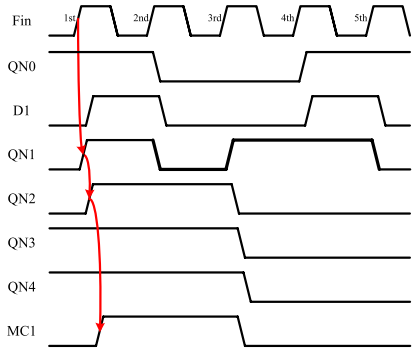

Fig. 4. Timing diagram of proposed divider-by-16/17 prescaler.

divide-by-3 operation in a cycle. By adopting the pseudo divide-by-2/3 prescaler, an OR gate is saved and there leaves only one AND gate in front of DFF0. As a result, the critical path #1 in conventional circuit is disappeared and the length of critical path #2 is reduced. Second, QN1 and QN2 node (instead of $Q1$ and $Q2$ node in conventional circuit) of DFF1, DFF2, and DFF3, is connected to the input CLK node of DFF2, DFF3, and DFF4, respectively. The propagation delay of DFF1, DFF2, and DFF3 will all decrease from t_{d_Q} to t_{d_QN}. Thus, the length of critical path will be further reduced.

The operation mode of proposed circuit is as follows. When MC = 1, MC1 changes its value according to (QN2, QN3, QN4). The pseudo divide-by-2/3 prescaler controlled by MC1 accomplishes seven times of divide-by-2 operations and one time of divide-by-3 operation in a cycle. The whole circuit operates in divide-by-17 mode. When MC = 0, MC1 keeps low and the pseudo divide-by-2/3 prescaler keeps on divide-by-2 operation. The whole circuit works in divide-by-16 mode.

As well as the conventional circuit, the maximum working frequency of proposed prescaler is decided by its divide-by-17 operation mode. In addition, the key operation in divide-by-17 mode is the divide-by-3 operation of pseudo divide-by-2/3 prescaler. Fig. 4 shows the timing diagram of this key operation of proposed circuit. In the first rising edge of Fin, QN1 and QN2 switch to high, then MC1 switches to high and holds for two periods. In the second rising edge, QN0 and D1 switch to low for two periods. In the third rising edge, QN1 switches to high and holds for two periods. From the second to the fifth rising edge of Fin, DFF1 outputs a divide-by-3 signal in node QN1 and the pseudo divide-by-2/3 prescaler accomplishes a divide-by-3 operation. After this, the pseudo divide-by-2/3 prescaler will carry out seven times divide-by-2 operation. A divide-by-17 signal will be obtained in node Fout.

Fig. 5 shows the MOSFET-level schematic of the proposed divide-by-16/17 prescaler. The whole circuit is realized in TSPC structure for high robustness and low static power. AND1 and AND2 are absorbed into the first stage of DFF0 and DFF1, respectively. Only normal MOSFETs are adopted in the circuit, the total cost can be saved. What's more, for the low voltage operation, the six cascoded MOSFETs may need to be split into several branches and each of that should have less number of cascoded MOSFETs. Thus, the correct function can be maintained.

From the timing analysis in Fig. 4, in the second rising edge of Fin, QN1 switches to low and then D1 switches to low no matter what the value of QN0 is. But QN0 has to be low in the third rising edge so that D1 can hold the low value for one more period. That means MC1 should switch to high at least before the third rising edge of Fin coming. From Fig. 4, MC1 starts to become high in the first rising edge. Signal should pass the MC1 path within two periods of Fin. The MC1 path is the critical path of proposed circuit as shown

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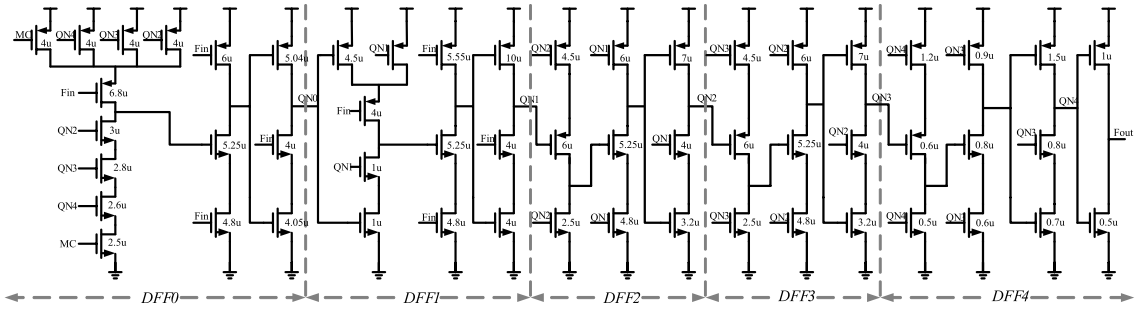

Fig. 5. MOSFET-level schematic of the proposed divide-by-16/17 prescaler ($L = 0.18\ \mu$m).

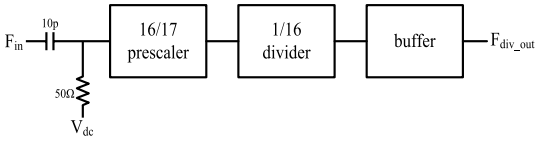

Fig. 6. Diagram of the on-chip testing configuration.

in Figs. 3 and 4. It comes through DFF1, DFF2, and AND1. The minimum period of the proposed divide-by-16/17 prescaler $T_{\text{min,pro}}$ can be written as

$$T_{\text{min,pro}} = \frac{t_{d\_\text{QN,DFF1}} + t_{d\_\text{QN,DFF2}} + t''_{\text{setup,DFF0}}}{2} \tag{5}$$

where $t_{d\_\text{QN,DFF1}}$ means the propagation delay from CLK to QN of DFF1; $t''_{\text{setup,DFF0}}$ means the setup time of DFF0 with absorbed AND1 gate, which is about a four-input NAND gate's delay.

The minimum working period of the conventional and proposed circuit, (4) and (5), can be compared as follows. $t_{d\_\text{QN,DFF1}}$ is about an inverter delay less than $t_{d\_Q,\text{DFF1}}$; $t''_{\text{setup,DFF0}}$ is a NOR gate's delay less than the sum of $t'_{\text{setup,DFF0}}$ and $t_{d,\text{NAND}}$. Thus

$$T_{\text{min,con}} - T_{\text{min,pro}} \approx \frac{t_{d,\text{NOR}} + t_{d,\text{INV}}}{2}. \tag{6}$$

By adopting a pseudo divide-by-2/3 prescaler, the minimum working period is reduced by half a NOR gate's delay. By changing the connection of TSPC DFFs, the minimum working period is further reduced by half an inverter's delay.

The speed improvement of the proposed circuit can be estimated as follow. Under the 0.18-μm standard CMOS process, the simulated maximum working frequency of conventional 16/17 dual modulus prescaler is ~4.5 GHz. It corresponds to a working period of 222 ps. Simulation results also show that an inverter's delay is ~45 ps and a NOR gate's delay is ~80 ps. Then, the minimum working period of proposed circuit will be reduced to 159.5 ps. The maximum working frequency of the proposed circuit is ~6.3 GHz, which is improved by ~40% when compared with the conventional circuit.

IV. Measurement Results

The proposed divide-by-16/17 prescaler is fabricated in an industrial 0.18-μm CMOS technology. Fig. 6 shows the diagram of the on-chip testing configuration. The input RF signal is fed through a 10-pF dc-blocking capacitor. The dc level of the input signal is configured by Vdc through a 50-Ω polyresistor, which is used for input impedance matching. The output frequency is scaled down by a fixed divider-by-16. This setup makes the output signal less vulnerable to the parasitic factors, such as pad capacitance, cable loss, and input capacitance of measurement equipments. Fig. 7 shows the micrograph of proposed circuit. The whole chip is ~0.73 mm × 0.69 mm.

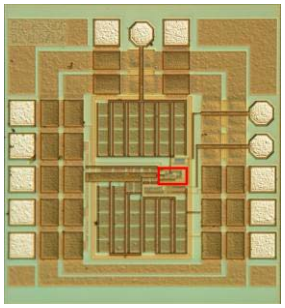

Fig. 7. Micrograph of proposed divide-by-16/17 prescaler.

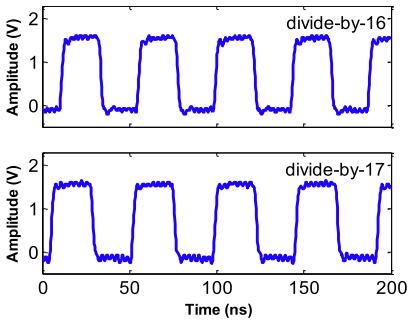

Fig. 8. Waveform of Fdiv_out at 5.8-GHz input frequency.

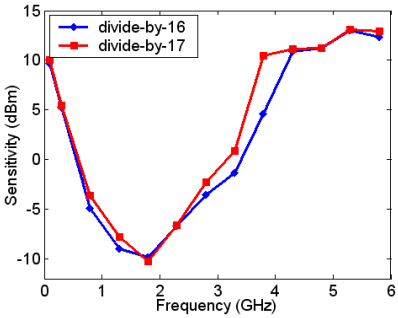

Fig. 9. Sensitivity versus working frequency of proposed circuit.

The circuit in the red rectangular is the core divide-by-16/17 prescaler circuit, which is only 0.04 mm × 0.08 mm.

Measurement results show that the proposed circuit achieves a maximum working frequency of 5.8 GHz under 1.6 V supply voltage. Fig. 8 shows the waveform of scaled output Fdiv_out with the maximum working frequency.

Fig. 9 shows the measured sensitivity versus working frequency in divide-by-16 and divide-by-17 modes. The two modes have similar characters of sensitivity variation with input frequency. The sensitivity is first decreased and then increase with input frequency.

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TABLE I
COMPARISON OF PROPOSED CIRCUIT WITH PREVIOUS WORKS

	[7]	[9]	[12]	[13]	[10]	[14]	This work
Publication	IEICE	TSCAS-II	EL	TMTT	TSCAS-I	TVLSI	-
Year	2012	2011	2008	2006	2010	2012	-
Type	TSPC	TSPC	IL	E-TSPC	TSPC	TSPC	TSPC
Divide ratio	2/3	7/8/9	55/56	8/9	32/33	32/33/47/48	16/17
Frequency	0.2~2.4	3.4~5	3.2~6.1	1.0~4.0	1.5~4.5	2.4~2.484	0.002~5.8
Power (mW)	0.7	1.6*	4.6	3.3	1.4	2.2	2.6
Supply (V)	1	1.2	1.8	1.8	1.8	1.8	1.6
Process (μm)	0.18	0.18	0.18	0.18	0.18	0.18	0.18

*simulation results

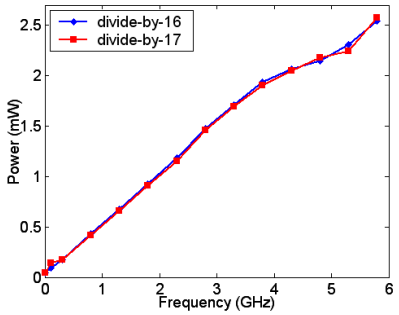

Fig. 10. Power versus working frequency of proposed circuit.

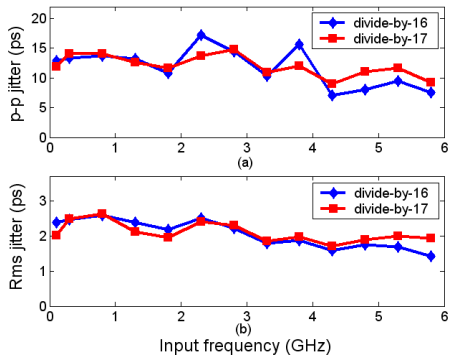

Fig. 11. Jitter performance of *F*div-out versus working frequency. (a) p–p jitter. (b) rms jitter.

Fig. 10 shows the measured power consumption of the proposed prescaler versus working frequency. The input signal is imported at its sensitivity level according to different frequency. The power increases linearly with input signal frequency and reaches ∼2.6 mW at the maximum working frequency (5.8 GHz). The power consumption in two modes is nearly the same at the same working frequency.

Fig. 11 shows the jitter performance of Fdiv_out versus input frequency. Both the p–p and rms jitters are slightly decreased when the working frequency increased. The average value is ∼10 and 2 ps for p–p and rms jitter performance, respectively.

Table I compares the proposed circuit with previous works, which focused on improving the speed of prescalers and implemented in CMOS technology. The maximum operating frequency of the proposed circuit is comparable with previous works. In addition, the proposed circuit achieves the widest working frequency range.

V. CONCLUSION

This brief presents a novel high-speed TSPC divide-by-16/17 dual modulus prescaler. The speed of the proposed circuit is improved in two aspects. First, by adopting a new pseudo divide-by-2/3 prescaler, the minimum working period is effectively reduced by half a NOR gate's delay. Second, by changing the connection of TSPC DFFs, the minimum working period is further reduced by half an inverter's delay. What's more, the minimum working frequency performance is not deteriorated at the same time. Fabricated in 0.18-μm CMOS technology, the proposed circuit achieves a 5.8-GHz maximum working frequency, and the measured working frequency range is from 2 MHz to 5.8 GHz. The power consumption is 2.6 mW at the maximum working frequency under 1.6 V supply voltage.

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