Novel Vedic Mathematics Based ALU Using Application Specific Reversibility

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***Abstract*—The proposed project utilizes the computational speed advantages of Vedic algorithm and energy optimization benefits of Reversible circuit. The Vedic algorithm optimizes the conventional mathematic computation logic used in the current processors thereby, effectively increasing the speed of computation. The Urdhva Triyambakam method derived from the ancient Indian mathematics will be used in the proposed project. Reversible circuits, on the other hand, reduces the power dissipation incurred due information/bits loss as in the case of an irreversible circuit making way for better power utilization along with reduced heat dissipation. The proposed project introduces the concept of application specific reversibility wherein the logical states belonging only to a particular function of the module is being considered, which significantly impacts in reducing the area limitations of a reversible unit while keeping its power efficiency benefits. The circuit design presented utilizes the above technique mentioned while designing the adder, multiplier along with other modules of an ALU.**

***Keywords*—Reversible, Semi-reversible gates, Vedic mathematics, Urdhva Triyambakam, Sutra.**

I. Introduction

The Primary objective of a digital circuit design is to optimize for speed, area, power and energy. While it's a challenge for circuit designers, to achieve this optimization without compensating for one or the other parameters mentioned above. Certain design techniques, algorithms and smarter planning of the available resources have proven to be successful to achieve the level of optimization required for much higher efficiency. Arithmetic Logic Unit (ALU) being the driving component of a processor, optimizing its module for speed and power becomes quite inevitable.

Many previously published technical papers have emphasized the use of reversibility in circuits design for reduction in power dissipation, while successfully demonstrating the same. However this reduction in power was also followed by significant reduction in speed as well as increase in chip area. Hence smarter algorithm and logic design was required to speed up the execution of a logic module. With this reference, 'Vedic Algorithm' technique was utilized to pave way for faster execution of an arithmetic module of an ALU.

While there are as many as 16 techniques(sutras) in the Vedic algorithm, the proposed design will implement multiplier using the popular Urdhva method (Urdhva Triyambakam) along with certain improvisation while designing the same, further details of which is explained in the subsequent parts of the paper. The conventional way of implementing the multiplier would have involved series of AND gates and adders to get the required output while incurring significant delay. The Vedic algorithm provides a faster way to get through the output with less number of logical elements involved, thereby reducing the delay while effectively increasing the speed of processing the output.

A simple illustration of Vedic technique is explained in the figure.

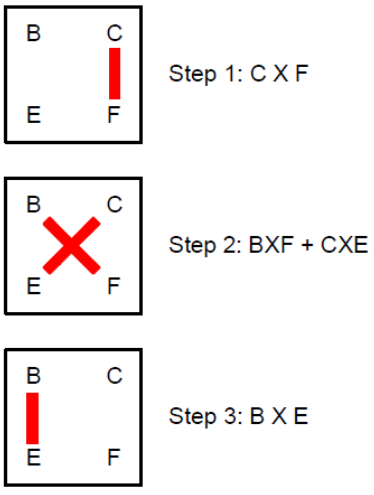

Fig. 1. Multiplication Technique Using Urdhva Triyambakam Sutra [1].

978-1-4799-6480-2/15/$31.00 © 2015 IEEE

II. REVERSIBLE COMPUTING

A. Reversibility

The strengths of Reversibility in digital circuits is well documented and explained by R. Launder [9] in his article. A circuit which can undo or reverse its output to get back its original input will not suffer information loss, since all the information are present within the circuit and only need to be reversed, to be recovered. Hence a reversible circuit will save major chunk of power dissipation suffered due to information loss that happens every clock cycle.

The basic requirements of a reversible circuit is to have a one-to-one correspondence between inputs and outputs, which requires the input and output pin count to be same. Also each input state must correspond to a particular unique state of the output i.e. output states cannot be shared by more than one input states available. If the above criteria are satisfied the inverse circuit can be easily designed to make the circuit reversible.

B. Application Specific Reversibility (Semi-Reversibility)

The proposed design introduces a concept of functionally reversible circuit. In the proposed multiplier module this reversibility is achieved by only considering only those states that occur in the n-bit multiplier inputs as well as outputs. By carefully mapping these states to a particular output and by adding required extra inputs this form of reversibility is achieved. However this circuit is not completely reversible and only reversible for the application required by the module to perform, hence this type of circuit manages to be partially or semi-reversible. The advantage of this design is that

- It requires less area compared to the previous multipliers which are implemented using basic reversible gates.
- It has less number of garbage bits.
- It has no constant input pin included which are generally used for making a general purpose reversible gate to an application specific one.

Hence it is a more efficient design.

C. Reversible Gates

The reversible gates used in this paper are as follows.

- Peres Gate

  Peres gate is a 3x3 reversible gate. The quantum cost of this gate is 4. It is mainly used for half adder application. It has lesser area and quantum cost compared to other reversible gates like Fredkin and Feynman gate. It has three inputs A, B and C. The outputs are given as P=A, Q=A⊙B and R=(A.B)⊙C. To use it as an half adder C is given logical zero. The outputs of the gate become P=A, Q=A⊙B and R=A.B.

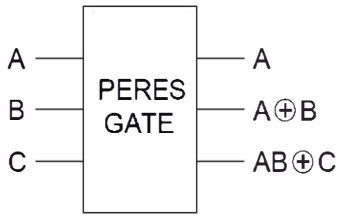

Figure 1. Peres Gate [8]

- HNG Gate

  HNG gate is a 4x4 reversible gate. It is mainly used for full adder application. The quantum cost of this gate is 6. It has four inputs A, B, C and D. The outputs are given as P=A, Q=B, R=A⊙B⊙C and S=(A⊙B).C⊙(AB⊙D). To use it as a full adder D is assigned to logical zero and C is assigned the input carry bit. The outputs of the gate become P=A, Q=B, R= A B C and S=(A⊙B).C⊙AB.

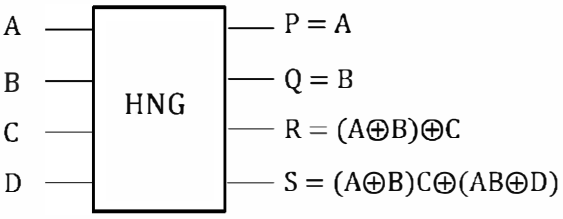

Figure 2. HNG Gate [5]

- BJN Gate

  It is a 3x3 reversible gate. The quantum cost of this gate is 5. For the three inputs A, B and C the outputs are P=A, Q=A and R=(A+B)⊙C. In this paper it is used in the logical unit. This gate is used to realize OR and NOR gates. When C=0, R=(A+B) and for C=1, R=(A+B).

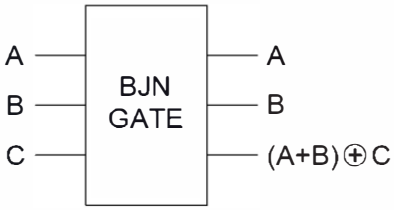

Figure 3. BJN Gate [6]

- TSG Gate

  It is a 4x4 reversible gate. This gate can realize most of the Boolean logical operations like AND, NAND, XOR, XNOR and NOT. The outputs of this gate are P=A, Q=A'C'⊙B', R=(A'C'⊙B')⊙D and S=(A'C'⊙B')D⊙ (AB⊙C). Inputs C and D are used as control signals to select the logical operation.

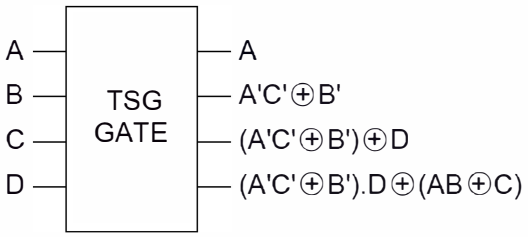

Figure 4. TSG Gate [7]

- Proposed KSA Gate

It is a 4x7 semi-reversible logic gate designed especially for 2-bit multiplication application. Out of the seven outputs, the first four outputs give the product of the two 2-bit inputs assigned to the four input pins. Three more output pins are added to make one-to-one mapping between inputs and outputs. Since this gate has 7 output bits it is expected to have one-to-one mapping between all the 128 cases. The proposed semi-reversible gate has one-to-one mapping between the inputs and outputs for the possible 16 cases of output product. Using a general purpose reversible gate for a specific application has more number of redundant gates and garbage outputs.

The conventional reversible 2-bit vedic multiplier uses six peres gates, four of which are used for AND operation and two for half adder application. Peres gate has two garbage outputs and two redundant gates when used for AND operation and one each for half adder application. The conventional 2-bit multiplier consists of 8 redundant gates and 8 garbage outputs.

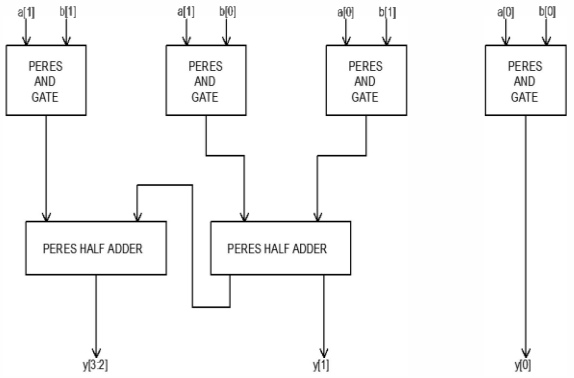

Figure 5. Conventional Reversible Vedic Multiplier [4]

The proposed KSA gate is optimized for 2-bit multiplication application. It has only 3 redundant gates and 3 garbage outputs. The total number of logical elements is lesser than the previous multipliers which saves the area on the chip. The performance of this gate is same as that of an ordinary 2-bit vedic multiplier.

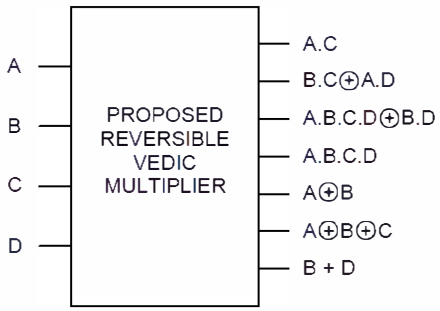

Figure 6. Proposed Semi-Reversible KSA Gate

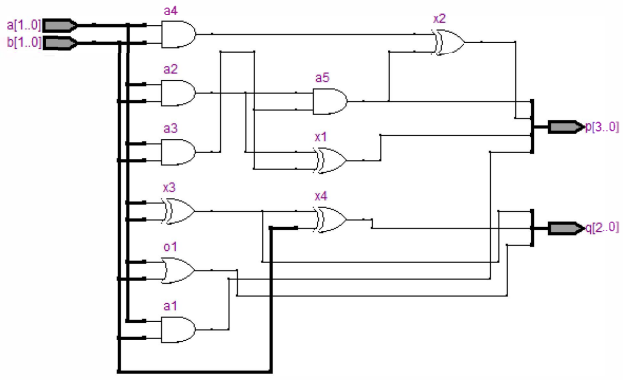

Figure 7. RTL Schematic of Proposed KSA.

III. ALU DESIGN

The proposed ALU design has a four bit control signal. It performs five arithmetic operations and eight logical operations. The proposed ALU uses both reversible and semi-reversible gates in it.

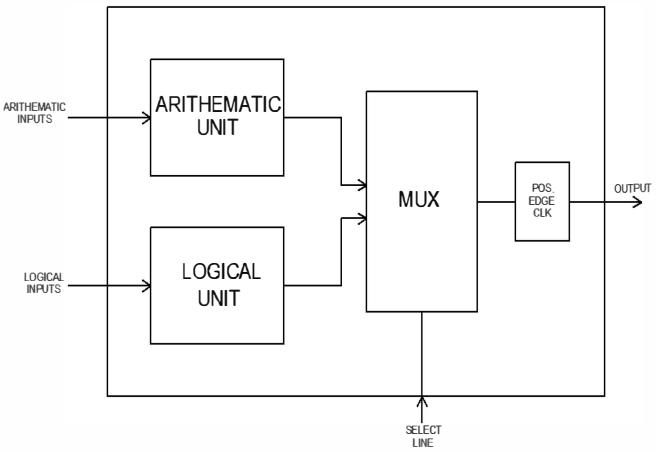

Figure 8. Proposed Architecture of ALU

The operations performed based on the control bits are as follows. Total of thirteen operations are performed by the proposed ALU.

TABLE 1. OPERATIONS PERFORMED BASED ON THE CONTROL SIGNAL.

Control Signal	Operation
0000	Addition
0001	Subtraction
0010	Multiplication
0011	Increment
0100	Decrement
0101	A.B
0110	A⊙B
0111	$\overline{A \odot B}$
1000	$\overline{B}$
1001	$\overline{A.B}$
1010	$\overline{A}$.B
1011	A+B
1100	$\overline{A+B}$

A. Full Adder/Subtractor

This adder is a 4-bit ripple carry adder. It is made using four HNG gates. HNG gates have the minimum delay, area and quantum cost for full adder application. The two inputs and carry bit is given to the first, second and third input respectively of the HNG gate. The fourth input pin of this HNG gate is grounded so it acts as a full adder. The output bits of the HNG will be P=A, Q=B, R=(A⊙B)⊙C, S=(A⊙B).C⊙AB. R is the sum of the addition and S is the carry. A control signal S is used to switch between adder and subtractor mode. When S=0, the circuit acts as a 4-bit full adder. When S=1, input b is complemented and an input high carry bit is given to the LSB full adder. In subtractor, R is the difference and S is the borrow bit. If the result of the 4-bit subtraction is negative then the borrow will be zero and output is stored as 2's complement.

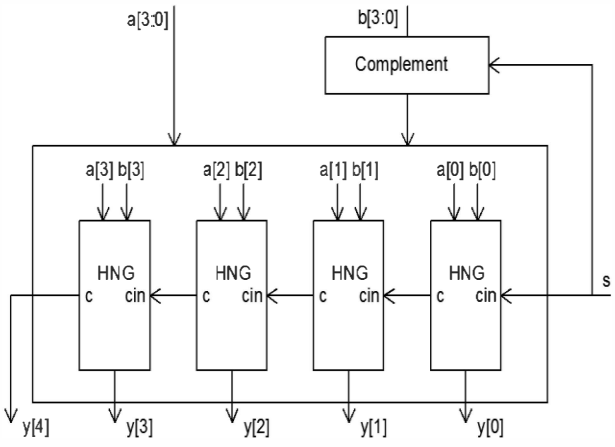

Figure 9. Reversible Full Adder/Subtractor

B. Vedic Multiplier

The circuit uses the proposed 2-bit semi reversible multiplier gate which uses lesser number of control input pins, lesser area and produces lesser number of garbage outputs compared to the 2-bit multiplier made using basic reversible gates. The four bit inputs are split into two parts of 2-bit each. For multiplication of 4-bit inputs, four 2-bit multipliers and three adders are required. Each part of input is multiplied with each part of the other input using the four 2-bit multipliers. This technique is represented in the following diagram.

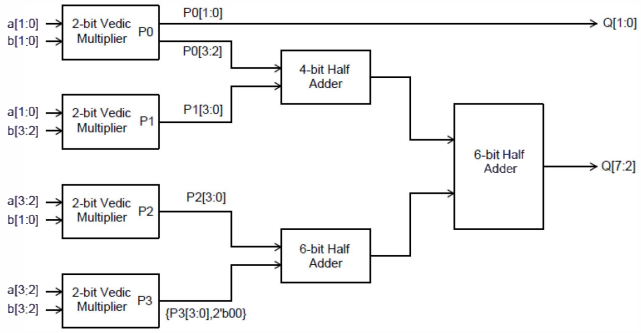

Figure 10. Reversible 4-bit Vedic Multiplier [1]

The last two bits of product of a[1:0] and b[1:0] is assigned to output q[1:0]. The first two bits are added to the product of a[1:0] and b[3:2]. The product of a[3:2] and b[1:0] is added by the left shifted by 2-bit product of a[3:2] and b[3:2]. The result of the these two addition is added to get output bits q[7:2]. This approach of multiplication is based on the vedic technique of multiplication called Urdhva Triyambakam Sutra. Multiplication of higher bits can be done in the similar manner. This multiplication technique is faster than any of the conventional multipliers and other vedic multipliers. This technique uses less number of computational steps to get the result. Since an optimized 2-bit semi-reversible is used area has been reduced compared to the previous vedic multiplier.

C. Logical Unit

The proposed 4-bit logic unit performs the logic operations on two 4-bit numbers. The 8 basic logic operations performed by proposed logic unit are AND, NOR, XNOR, XOR, NOT (invert), NAND, A'B, OR, NOR etc. A BJN gate is used to implement OR and NOR operations. A control input C controls the operation of a BJN gate. When C=0, BJN gate performs OR operation of two inputs A and B. When C=1, it gives NOR operation of A and B. TSG gate is used to implement the rest of the logical operations. Input C and D acts as control signals to TSG gate. When C=0 and D=0, it results in AND operation of A and B. When C=0 and D=1, it gives XOR and XNOR operations of A and B. When C=1 and D=0, the resulting output is inversion of B and NAND operation of A and B. When C=1 and D=1, it results in A'B. Thus overall logic unit uses only two types of reversible gates to implement 8 logic operations so as to reduce the complexity and power.

IV. Analysis

The FPGA was implemented in Stratix II family with model number EP2S15F484C5. The comparative results of the proposed ALU to the previous ALU is as follows.

TABLE 2. COMPARATIVE RESULTS OF 2-BIT MULTIPLIER

Parameter	**Previous 2-bit Vedic Multiplier**	**Proposed 2-bit Vedic Multiplier**	**% change**
Combinational ALUT (Area)	10	7	30% decrease
Total Thermal Power Dissipation(mW)	384.32	355.39	7.6% decrease
Total pins	18	11	39% decrease
Worst-case Delay(ns)	13.726	14.310	4.25% increase

TABLE 3. COMPARATIVE RESULTS OF 4-BIT MULTIPLIER

Parameter	**Previous 4-bit Vedic Multiplier**	**Proposed 4-bit Vedic Multiplier**	**% change**
Combinational ALUT (Area)	54	40	26% decrease
Total Thermal Power Dissipation(mW)	619.11	481.75	22% decrease
Total pins	85	57	33% decrease
Worst-case Delay(ns)	14.653	14.310	2.3% decrease

V. Conclusion

The proposed design presented, successfully establishes the power and area advantages brought forward by Selective Reversal as well as faster algorithm based on Vedic Method. The reduced state requirements directly contributed to reduced pin count (33% decrease) and the area of the chip (decreased area requirements by 26%). Semi-Reversibility also proved to be power efficient than the previous similarly proposed reversible unit (reduction in power of 22%). This was the first time wherein the impact of semi-reversibility was proposed demonstrated and detailed. The technique can also be applied for any other reversible circuit designing, where the area and power requirements are stringent.

Acknowledgment

The authors would like to thank for the help and guidance received to them by Prof. R Dhanabal (Asst. Prof, VLSI Sense, VIT).The proposed work was partially supported by VLSI Sense Division of VIT University, Vellore.

References

[1] Mr. Abhishek Gupta, Mr. Utsav Malviya, Prof. Vinod Kapse, "Design of Speed, Energy and Power Efficient Reversible Logic Based Vedic ALU for Digital Processors", IEEE, 2014.

[2] W. David Pan, Mahesh Nalasani, "Reversible Logic", IEEE Potentials 0278-6648/05© 2005 IEEE.

[3] Jagadguru Swami Sri Bharati Krishna Tirthji Maharaja,"Vedic Mathematics", Book, Motilal Banarsidas, Varanasi, India, 1986.

[4] Rakshith TR., Rakshith Saligram, "Design of High Speed Low Power Multiplier using Reversible logic: a Vedic Mathematical Approach", International Conference on Circuits, Power and Computing Technologies [ICCPCT-2013].

[5] Matthew Morrison, Nagarajan Ranganathan, "Design of a Reversible ALU based on Novel Programmable Reversible Logic Gate Structures", 978-0-7695-4447-2/11 © 2011 IEEE.

[6] Nagamani A N, Jayashree H V, H R Bhagyalakshmi, "Novel Low Power Comparator Design using Reversible Logic Gates", Indian Journal of Computer Science and Engineering (IJCSE), ISSN : 0976-5166, 2011.

[7] Himanshu Thapliyal, M.B Srinivas, "A New Reversible TSG Gate and Its Application For Designing Efficient Adder Circuits", 0-7803-9283-3, IEEE Bangkok, 2005.

[8] Prashant .R.Yelekar, Prof. Sujata S. Chiwande, "Introduction to Reversible Logic Gates & its Application", 2nd National Conference on Information and Communication Technology (NCICT) 2011, Proceedings published in International Journal of Computer Applications® (IJCA).

[9] R. Landauer, "Irreversibility and Heat Generation in the Computational Process", IBM Journal of Research and Development, 5, pp. 183-191, 1961.