DESIGN AND TESTING OF COMBINATIONAL LOGIC CIRCUITS USING BUILT IN SELF TEST SCHEME FOR FPGAs

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Abstract— **In Very Large Scale Integration (VLSI), while manufacturing IC, Test time and cost plays a very significant role. If faulty components find during IC manufacture then cost increases. So it is essential to minimize test time and cost. In this paper Built In Self Test (BIST) architecture is designed for testing combinational logic circuits and fault models like stuck at one and stuck at zero are tested, simulated and validated using Spartan 6 FPGA and Xilinx ISE 14.2 tool. BIST architecture with fault and without fault in circuit under test is compared for the parameters such as area, memory, delays time and device utilization.**

Keywords— BIST; LFSR; MISR; CUT; S-A-1; S-A-0;

I. INTRODUCTION

With the ever-increasing complexity and density of present day integrated circuits, the cost of testing has become a significant part of the overall product. Thereby, Built-In Self-Test (BIST) has been proposed as a powerful design for testability technique for addressing the highly complex testing. BIST design includes on-chip/board circuitry to provide test patterns and to analyze output responses. It can perform the test internal to the chip so that the need for complex external testing equipment is greatly reduced. Using BIST many of the traditional testing problems (low accessibility of internal nodes that increases the test complexity) can be overcome [1].

Another interesting feature of BIST strategies is that it allows rapid testing of the circuit. The test is performed at the nominal operation frequency without resorting to an external high speed tester that represents an expensive Automatic Test Equipment (ATE) and which additionally does not always have a timing accuracy comparable to the IC internal speed on the boards.

BIST reduces testing costs. In order to understand why, consider the example of a 1 GHz microprocessor on a chip with 800 pins. For reliable stuck-fault and limited transition-delay fault testing, we should conduct the test at the rated clock speed. This forces us to use the Advantest Model T6682 1 GHz ATE, which can sample circuit outputs at this rate. The Tester costs 800 pins × $6,000 per pin = $ 4,800,000, but there is no chip area cost due to testing, because we do not use on-chip BIST hardware. BIST reduces testing costs. In order to understand why, consider the example of a 1 GHz microprocessor on a chip with 800 pins. For reliable stuck-fault and limited transition-delay fault testing, we should conduct the test at the rated clock speed. This forces us to use the Advantest Model T6682 1 GHz ATE, which can sample circuit outputs at this rate. The tester costs 800 pins × $6,000 per pin = $ 4,800,000, but there is no chip area cost due to testing, because we do not use on-chip BIST hardware.

Therefore, there is a huge initial capital cost for the ATE, but there is no recurring chip area cost on each chip for test hardware. If, instead, we provide BIST hardware, then the need for a very high-speed ATE is eliminated, except to test the wires from the circuit pins to the Input MUX, and from the circuit outputs to the output pins. The number of tests for that is very short, say perhaps 7 or 8 patterns and measurements per pin, and the cost of this can be safely ignored in this analysis. Therefore, with BIST doing all stuck-fault and transition delay fault testing, we need a 1 GHz signal oscillator to clock the chip, and we need the ATE only to provide DC command signals to tell the microprocessor to perform BIST. Finally, we need an ATE to read out the success or failure DC signal for BIST from a circuit pin. In this case, we can use an inexpensive, 20 MHz ATE that costs roughly $391 per pin, so our cost is 800 pins × $391 per pin = $312,800, a savings of $4,487,200. This example is hardly far fetched. On-chip clock rates are expected to rise above 1 GHz, and at present, no ATE exists to test a circuit above 1 GHz [2].

II. BIST ARCHITECTURE

Built in self test is a design for testability (DFT) technique in which testing is carried out using built in hardware features. Advantage of this methodology is that the test patterns are not applied by external Automatic Test Equipments (ATEs) but generated by inbuilt testing circuit. It saves the memory requirement during test. A typical BIST architecture consists of a test pattern generator (TPG), usually implemented as a linear feedback shift register (LFSR), a test response analyzer (TRA), implemented as a multiple input shift register (MISR), and a BIST control unit (BCU), all implemented on the chip as shown in Figure 1[2]. This approach allows applying at-speed

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tests and eliminates the need for an external tester. The BIST architecture components are given below [13].

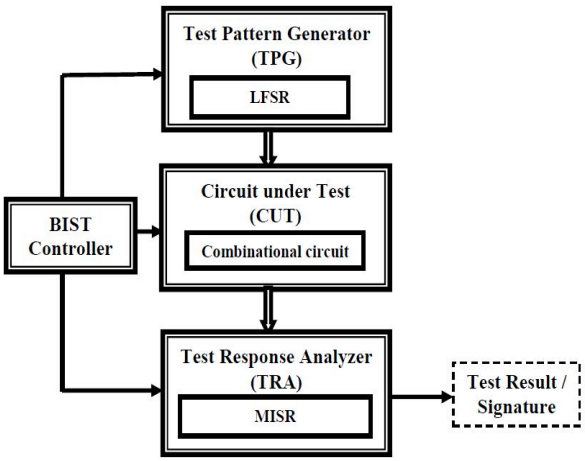

Figure 1: Basic block diagram of a BIST

- Test pattern Generator (TPG): Test pattern generator (TPG) generates the test patterns for CUT. It is a dedicated circuit or a microprocessor. The patterns may be generated in pseudorandom or deterministically [8].
- Circuit under Test (CUT): Circuit under Test (CUT) is the portion of the circuit tested in BIST mode. It can be sequential, combinational or a memory.
- Test Response Analyzer (TRA): Test Response Analyzer (TRA) analyses the value sequence on primary output and compares it with the expected output BIST controller unit. It controls the test execution; it manages the Test pattern generator (TPG), Circuit under Test (CUT), Test Response Analyzer (TRA) and reconfigures the CUT. It is activated by the normal/test signal and generates a go/no go.
- Multiple Input Signature Register (MISR): Multiple Input Signature Register(MISR) is designed for signature analysis which is a technique for data compression. MIPS are frequently implemented in BIST designs, in which output responses are compressed by MISR. MISR efficiently map different input streams to different signatures with every small probability of alias.

III. PROPOSED DESIGN METHODOLOGY

A. Linear Feedback Shift Register

LFSR is a shift register whose input bit is a linear function of its previous state [9]. The most commonly used linear function of single bits is XOR. Thus, an LFSR is most often a shift register whose input bit is driven by the exclusive-or (XOR) of some bits of the overall shift register value. Pseudo random number sequence generator [8] is generated in HDL according to the following circuit based on the concept of shift register as shown in Figure 2[3][4]. Combinational circuit in CUT requires only 3 inputs. 3-bit LFSR is sufficient for the implementation of TPG [5].

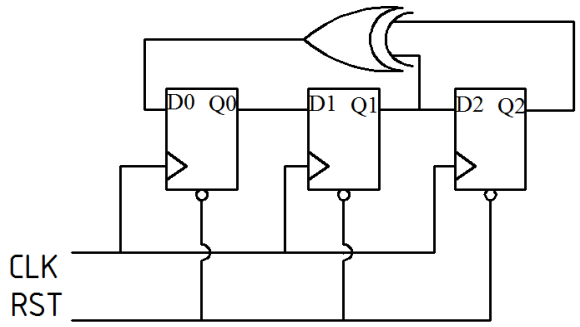

Figure 2: Circuit diagram of 3 bit LFSR

B. Circuit Under Test(CUT)

In this paper circuit under test is a combinational circuit show in the figure 3. The different types of test carried are with respect to Stuck-at fault. It means that the fault is modeled by assigning a fixed (0 or 1) value to a single line in the circuit (in this case 1st NAND gate). A single line is an input or an output of a logic gate or a flip-flop. Stuck-at fault can be derived into two parts one is single stuck-at fault another one is multiple stuck-at faults, a stuck-at fault is assumed to affect only the interconnection between gates.

However, multiple fault diagnosis becomes increasing difficulty and time-consuming as the size of integrated circuit increases. Many of methods have been introduced for diagnosing and deducing fault locations multiple faults in combinational circuit such as effect-cause analysis, guided-probing, analysis by forward propagation and backward implication using randomly generated input-pairs[8], analysis and diagnosis using both electron beam and LSI tester.

We have proposed methods to deduce suspected faults by algorithmically-generated sensitizing input-pairs without probing internal lines. To reduce the number of suspected faults, single and multiple fault simulation with diagnostic tests that lead to fault-free responses are used to identify non existent faults. To avoid missing actual faults in a fault circuit the proposed method uses the result of multiple fault simulation to diagnose multiple stuck-at faults. On the assumption that all suspected faults are equally likely in the faulty circuit, multiple faults simulations are performed.

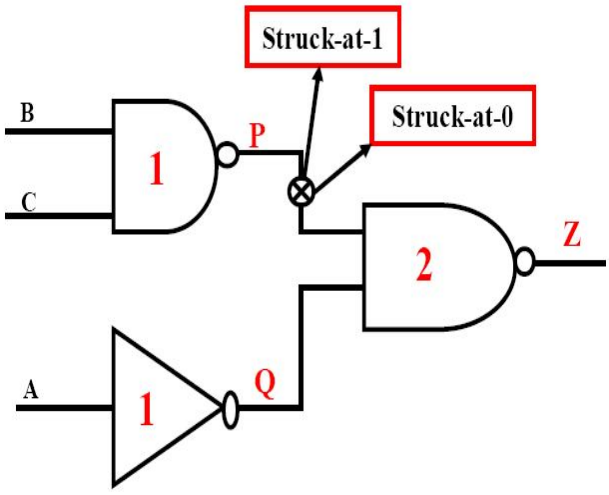

Figure 3: Flow chart of CUT

C. Multiple Input Signature-analysis Register (MISR)

A Multiple Input Signature-analysis Register (MISR) is one which can be used to reduce the amount of hardware required to compress a multiple bit stream. The MISR provides an alternative to using multiple Linear Feedback Shift Registers (LFSRs) in parallel and separately comparing the error polynomials. Test patterns for BIST can be generated at-speed by an LFSR with only a clock input. Then the outputs of the CUT (Circuit under Test) must be compared to the known good response which is termed as the golden signature. Signature analysis is the most popular compaction technique used today. Multiple input signature register (MISR) is the solution that compact all outputs into a single LFSR. It works because LFSR is linear and obeys superposition principle. All responses are superimposed into one LFSR. The final remainder is the XOR sum of remainders of polynomial divisions of each Primary Output by the characteristic polynomial. Its output develops a signature based on the effect of all the bits fed into it. If any bit is wrong, the signature will be different from the expected value and a fault will have been detected[6].

A Single-Input Signature Register (SISR) has been designed for this project. There are several ways to connect the inputs of LFSRs to form an SISR. Since the XOR operation is linear and associative, (A Xor B) Xor C = A Xor (B Xor C), as long as the result of the additions are the same then the different representations are equivalent. If we have an n -bit long SISR we can accommodate up to n inputs to form the signature. If we use m < n inputs we do not need the extra XOR gates in the last n – m positions of the SISR. SISR reduce the amount of hardware required to compress a multiple bit stream. LFSR and/or SISR circuit is implemented using a memory already existing in a circuit to be tested. If we apply a binary input sequence to LFSR, the shift register will perform data compaction (or compression) on the input sequence [11].

At the end of the input sequence the shift-register contents, Q0, Q1, and Q2, will form a pattern that we call a signature. If the input sequence and the serial-input signature register (SISR) are long enough, it is unlikely (though possible) that two different input sequences will produce the same signature. If the input sequence comes from logic that we wish to test, a fault in the logic will cause the input sequence to change. This causes the signature to change from a known good value and we shall then know that the circuit under test is bad. This technique, called signature analysis, was developed by Hewlett-Packard to test equipment in the field in the late 1970s. The simplest form of this technique is based on a single input LFSR [11].

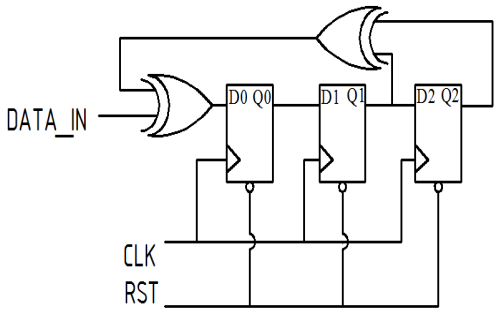

Figure 4: Circuit diagram of 3 bit Single Input Signature Register (SISR)

We can combine the PRBS generator of Figure 2 together with the signature register of Figure 3 to form the simple BIST structure for testing combinational circuit shown in Figure 3. LFSR generates a maximal-length ($2^3 - 1 = 7$ cycles) PRBS. MISR computes the signature of the CUT with s-a-1. LFSR is initialized to '101' (a = 1, b = 1, c = 1) and MISR is initialized to '101'. The schematic in Figure 5 shows how the TPG and TRA are used for testing CUT to s-a-1& s-a-0 fault. Table I shows how the bit sequences are calculated in the good circuit. The signature is formed in MISR and compared with circuit under test. We can observe the change in bits for MISR output, because of s-a-1 and s-a-0 faults present in the combinational circuit.

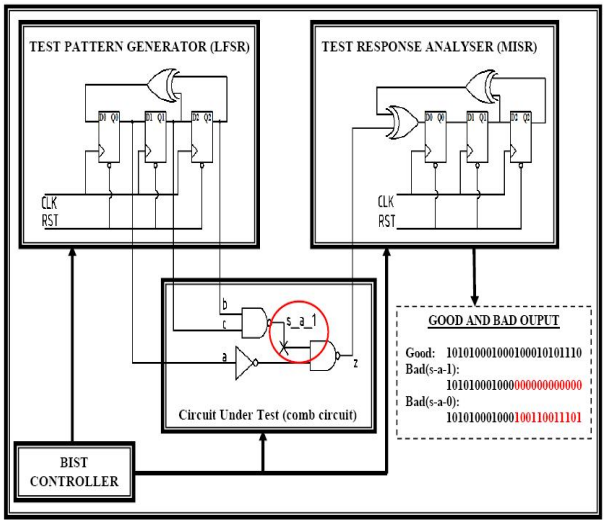

Figure 5: Circuit diagram of proposed BIST Architecture [11]

The MISR output with good circuit response as 10101000100010001010110. If s-a-1 fault is present at the input of second NAND gate the MISR output response changes to 10101000100000000000000 and because of s-a-0 fault presence the MISR output response changes to 10101000100010011011101.

TABLE I: BIT SEQUENCES OF PROPOSED BIST ARCHITECTURE

INPUTS			OUTPUT							
a	b	c	Without fault			With S-A-1 fault			With S-A-0 Fault	
1	1	1	1			1			1	
1	1	0	1			1			1	
1	0	1	1			1			1	
1	0	0	1			1			1	
0	1	1	1			0			1	
0	1	0	0			0			1	
0	0	1	0			0			1	
0	0	0	0			0			1	
MISR o/p without fault	101	010	001	000	100	010	101	110		
MISR o/p with s-a-1 fault	101	010	001	000	000	000	000	000		
MISR o/p with s-a-0 fault	101	010	001	000	100	110	011	101		

IV. RESULTS AND DISCUSSION

In this paper BIST architecture has been designed for combinational circuit using Spartan 6 FPGA and Xilinx ISE 14.2 tool.

First the 3-bit LFSR simulation result using XILINX 14.2 tool is observed by applying input signals Clock and Reset. 2^3 random pattern sequences are generated at the output signal. Then MISR simulation result using XILINX 14.2 tool is evaluated by inputting signals Clock, Reset and data_in (output signal from CUT for BIST design). 2^3 random pattern sequences are generated at the output signal.

Figure 6 (a) shows the BIST design output for CUT without fault. Clock and reset are the 2 inputs and data_out is an output signal for the top module. The combinational circuit under test is having input from LFSR and output is connected to MISR.

Output sequences –111 110 101 *011 110 101 010 100 001 001*

Figure 6 (b) shows the BIST design output for CUT with fault. Clock and reset are the 2 inputs and data_out is an output signal for the top module. The combinational circuit under test is having stuck at fault because of that the change in the output is

Output sequences –111 110 101 *010 101 010 101 011 111 110*

Figure 6(a): Simulation of BIST Architecture without Fault

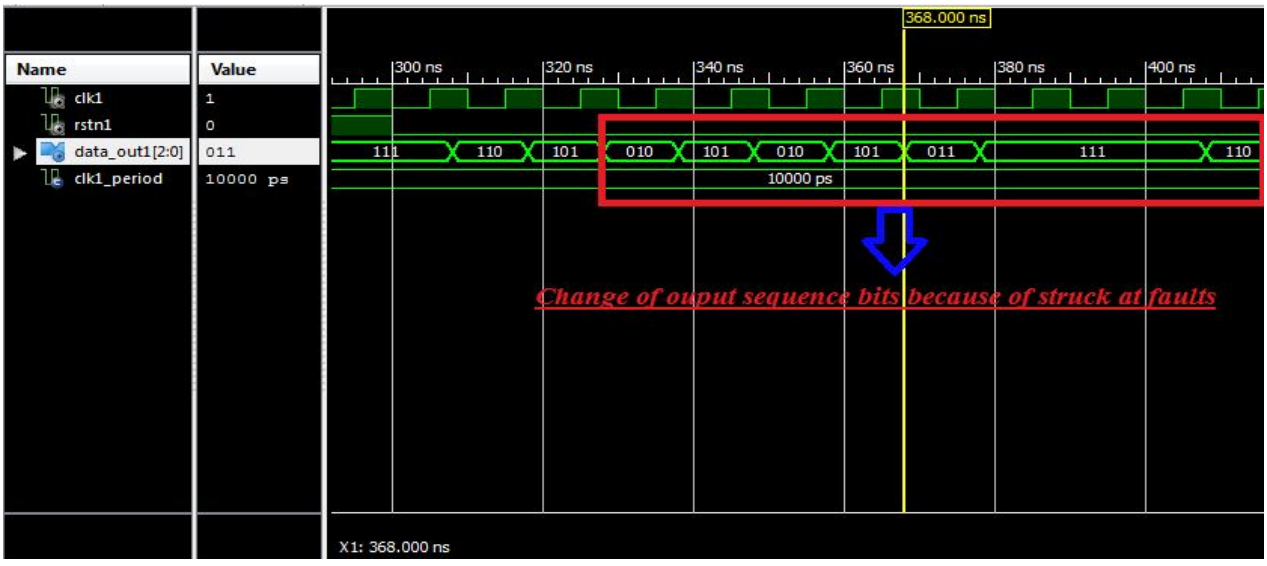

Figure 6(b): Simulation of BIST Architecture with Fault

TABLE II: PERFORMANCE COMPARISON

Parameters	BIST for CUT with Fault	CUT with fault	BIST for CUT without Fault	CUT without fault
Clock period	1000 ps	1000 ps	1000 ps	1000 ps
Memory Usage	187616 KB	188116KB	187232 KB	187992KB
Levels of Logic	1	2	2	3
Real time	4.00 s	4.00 s	3.00 s	5.00 s
CPU time	4.54 s	4.04 s	3.55 s	5.16 s
Time for simulation	10 ns	10ns	10 ns	10ns
Delay	2.690 ns	7.266 ns	3.536 ns	5.385 ns
Power	0.029 w	0.029 w	0.029 w	0.029 w

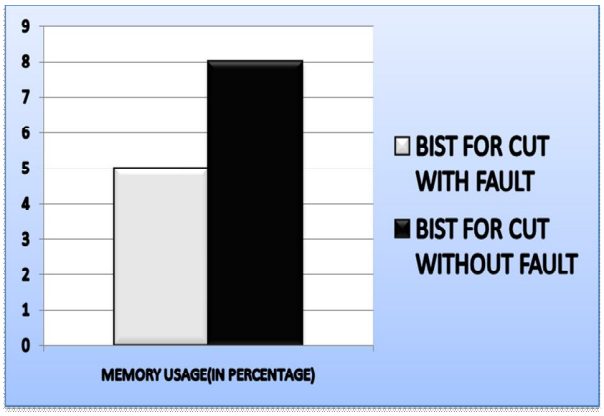

Figure 7(a): Graphical representation of Memory usage of BIST Design

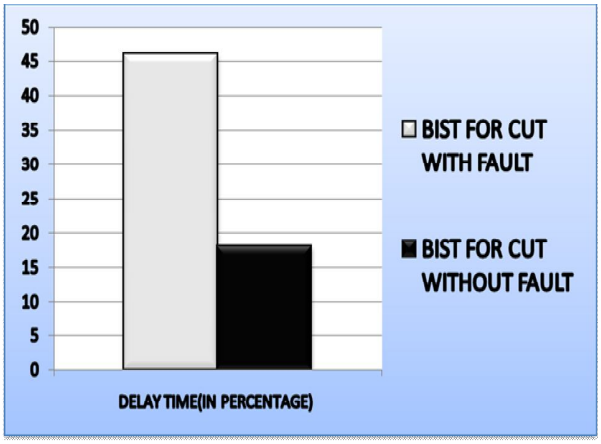

Figure 7(b): Graphical representation of Delay Time of BIST Design

CONCLUSION

In this paper BIST architecture has been designed for combinational circuit using Spartan 6 FPGA and Xilinx ISE 14.2 tool. Memory usage, Delay time reductions because of BIST design into CUT with fault and without fault are 5%, 8%, 46% and 19% respectively. Memory usage with BIST consumes lesser area when we compare with CUT with/without fault. Delay time without BIST takes longer time to complete execution of required result. By seeing these little variations in parameters justifies the BIST technique for combinational circuit will not affect the area overhead, memory issues and power consumption.

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