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Design and FPGA Implementation of Optimized 32-Bit Vedic Multiplier and Square Architectures

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Abstract—This paper presents the design of high speed multiplier and squaring architectures based upon ancient Indian Vedic mathematics sutras. In existing Vedic multiplier architectures, the partial product terms are computed in parallel and then added at the end to get the final result. In this work, all the partial products are adjusted using concatenation operation and are added using single carry save adder instead of two adders at different stages. The high speed Vedic multiplier architecture is then used in the squaring modules. The reduced number of computations in multiplication due to adjusting using concatenation operation and one carry save adder only, the designed multiplier offers significant improvement in speed. The designed architectures are realized using Xilinx Spartan-3E FPGA. The comparison shows the 28.72% and 38.59% reduction in propagation delay for the designed 32-bit multiplier as compared to the existing multiplier designs.

Keywords—VLSI, Vedic,* Urdhava-Tiryakbhayam, Dwandwa-yoga, *Multiplier, Square, IXI.

I. INTRODUCTION

The word '*Vedic*' was driven from the word '*Veda*' which is ancient store-house of all knowledge. Vedic mathematics provides the solution to the problem of long computation time by reducing the time delay needed for the operations to be performed. It has originated from "*Atharva Vedas*" the fourth Veda. *Atharva Veda* mainly deals with the branches like engineering, mathematics, sculpture, medicines and all other sciences. *Vedic* mathematics deals with all areas of mathematics either it is pure or applied. It was rediscovered from the Vedas between 1911 and 1918 by Sri Bharati Krishna Tirtha Ji. *Vedic* mathematics has been formulated on sixteen sutras and thirteen sub-sutras. These sutras offer magical short cut methods to all basic mathematical operations. All the advantages drives from the fact that *Vedic* mathematics approach is totally different & considered very close to the way a human mind works. *Vedic* mathematics can be applied to every branch of mathematics including arithmetic, algebra and geometry. The powerful applications of *Vedic* mathematics are in fields of Digital Signal Processing (DSP), Chip Designing, Discrete Fourier Transform (DFT), High Speed Low Power VLSI Arithmetic and Algorithms and encryption systems [1].

Arithmetic Logic unit (ALU) is the important unit in processors that performs basic arithmetic operations like addition, subtraction, multiplication and logical operations. Today's processors operate at very high clock speeds. Hence it is imperative to have faster additions, multiplications, squaring, and cubing etc. operations. Multiplication is the most basic & frequently used operation in ALUs. It is an operation of scaling one number by another. Multiplication operations also form the basis of other complex operations such as squaring, cubing, convolution, fast-Fourier transforms etc. Multiplication is the most time consuming amongst the basic mathematical calculations performed by arithmetic units. With these considerations, it is always important to have fast and efficient mechanism to implement multiplication function. Therefore, circuit designers are looking forward for new algorithms & methods to speed up all the arithmetic operations [2]-[8].

This paper illustrates design and implementation of high speed multiplier and square modules. These Vedic mathematics based modules along with other modules can be integrated in an ALU. This *Vedic* ALU will be far more efficient than the conventional one.

II. VEDIC MULTIPLIER ARCHITECTURE

This section introduces multiplication operation using *Vedic IXI Methodology* and then illustrates architecture of 2x2 multiplier module and finally architecture of n-bit multiplier. *Urdhava-Tiryakbhayam* sutra has been used for multiplication purpose. The fig. 1 explains multiplication of two decimal numbers using IXI technique:-

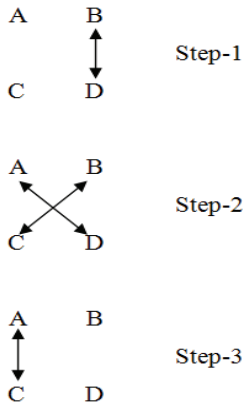

Fig. 1. IXI Methodology for Multiplication [1]

In this method initially multiplication of the rightmost digit of multiplier is performed with the rightmost digit of the multiplicand giving the LSB of the product term as shown in step-1 of fig. 1. Then multiplication of the leftmost digit of the

multiplicand with the rightmost digit of the multiplier and the rightmost digit of the multiplicand with the leftmost digit of multiplier is performed and then added. Thus forming the middle part of the product term as in step-2 of fig.1. At the last step, in step-3 the leftmost part of the multiplicand is multiplied with the leftmost part of the multiplier forming the leftmost part of the product term. In this way the multiplication process is carried out. Similar logic of cross-multiplication and addition can be extended to implement any number of bits. Each iteration gives the coefficient of the final product [1].

A. 2x2 Multiplier Module

The 2x2 multiplier module can be implemented using four AND Gates and two Half-adder modules and is shown in fig. 2. The total delay for 2x2 multiplier is only two half-adder delay.

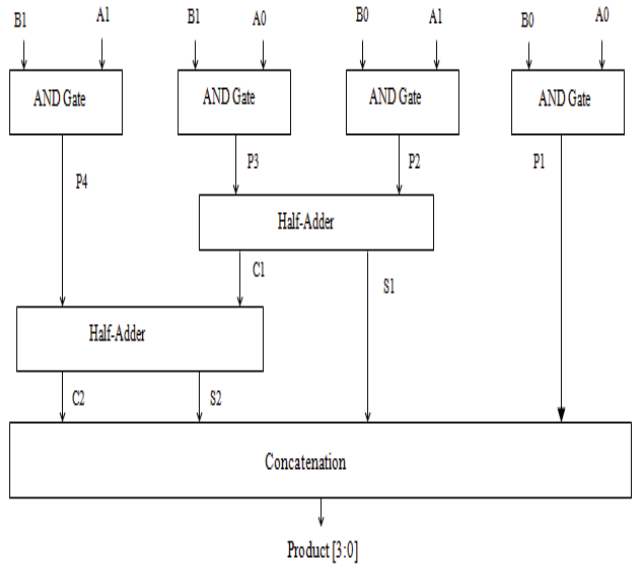

Fig. 2. Architecture of 2x2 Multiplier Module

It consists of four AND gates used for AND operation of single bit numbers, two half adders for the addition of numbers obtained in the previous section to provide the sum and carry. At the end concatenation of all the final results is done to obtain the final product of 4-bits.

This architecture is basically implementation of IXI technique. Firstly, right most digits are multiplied to give the LSB of the final product. Then LSB of first digit is multiplied with the MSB of second digit and MSB of first digit with the LSB of the second digit and are added together using the half adder block. The sum obtained from this adder block is the second digit of the product. At the next step MSB's of both the numbers are ANDed together and the result is added with the previous carry through half adder. So, the obtained sum makes the third digit of the final product and the carry will be the MSB of the product.

B. n-bit Vedic Multiplier Module

The architectural concept of n-bit Vedic Multiplier is shown in fig. 3. This architecture consists of four n/2 bit multipliers used for calculating the partial products. Next, the results of these n/2 bit multipliers are adjusted using concatenation operation to have all the partial product terms of equal bit-length. The partial product of right most multiplier is concatenated with the partial product of leftmost multiplier and the partial products of middle two multipliers are concatenated with (n/2) zeroes each.

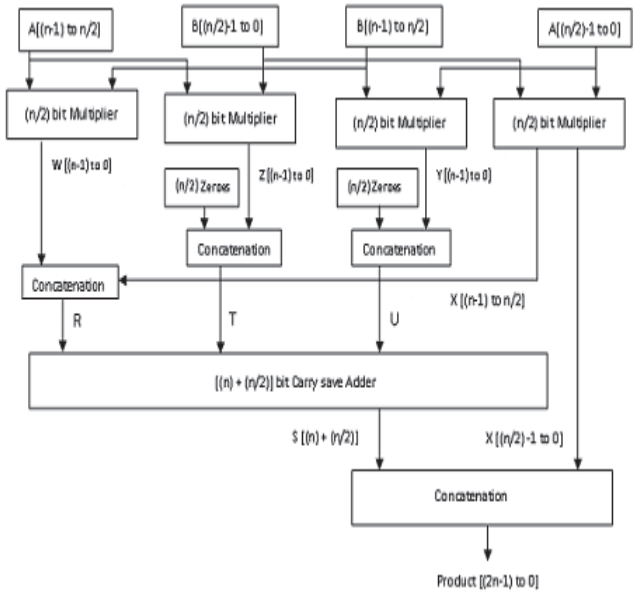

Fig. 3. Architecture of n-bit Multiplier

All the numbers obtained after concatenations are added together using the single carry save adder. At the end, the sum obtained from the carry save adder is concatenated with the LSB partial product of right most multiplier to get the required final product [11, 12], [14].

III. SQUARING ARCHITECTURE

Squaring is also the fundamental arithmetic operation to be performed. For squaring of a number *Urdhava-Tiryakbhyam sutra* along with *Dwandwa-yoga* is used. In this 'Duplex' technique is used. In the Duplex (D), twice the product of the outermost pair is calculated, and then added with twice the product of the next outermost pair, and so on till no pairs are left. When there is odd number of bits in the original sequence, there is one bit left in the middle, and this is entered as its square.

For 1-bit number (X0), D = X0 * X0.
For 2-bit number (X0X1), D = 2*X1*X0.
For 3-bit number (X2X1X0), D = 2 * X2 *X0 + X1 *X1.
For 4-bit number (X3X2X1X0), D = 2 * X3 * X0 + 2 * X2 * X1.

For finding the square the duplexes are calculated starting from the either side may be left or right and is proceeded to the other direction and vice-versa. At the end duplexes are added to get the final result [9, 10], [13], [15, 16].

A. 2-bit Squaring Circuit

For calculating the square of 2-bit number one AND gate and one Half-adder are used as shown in fig. 4.

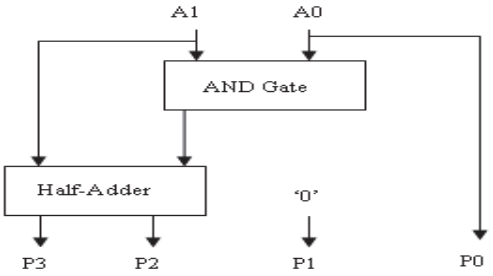

Fig. 4 Architecture of 2-bit Squaring Circuit

The LSB of the input is directly taken as the LSB of the final output. The next bit of the output will always be '0'. So, it is by default set to zero value always. Then both the inputs are ANDed together. The result is added to the MSB of the input numbers. The sum of the half-adder is taken as the third bit of the final result and the carry bit of the half-adder is the MSB of the final output. Thus, we get the final output of 4-bit for squaring module of two-bit number. This two-bit squaring circuit is the base circuit for developing the n-bit squaring module.

B. n-bit Squaring Circuit

The architecture for n-bit squaring module is shown in fig. 5.

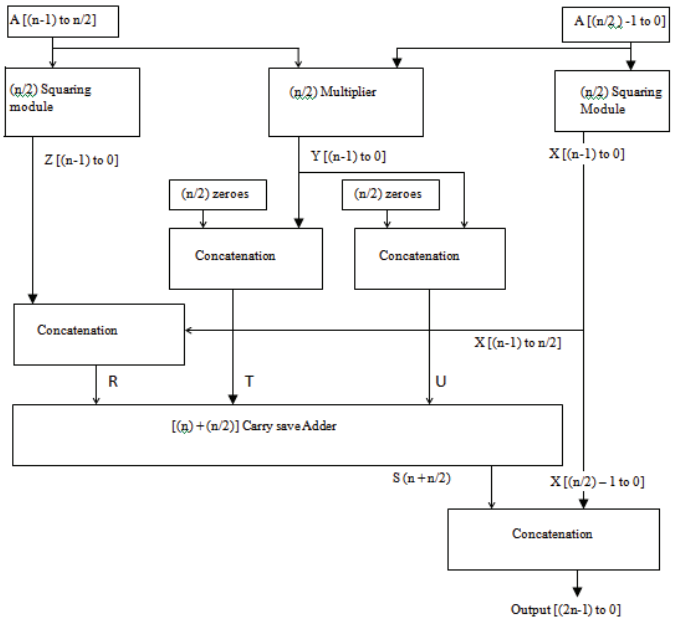

Fig. 5 Architecture of n-bit Square module

In this architecture, one multiplier of n/2 bits along with two squaring circuits of n/2 bits is used for the calculation of the partial products. At the last step all the calculated partial products are adjusted accordingly and are added together using the single carry save adder to get the final output.

IV. Simulation Waveform and Results

In this work 4-bit, 8-bit, 16-bit and 32-bit Vedic multiplier and squaring architectures are designed and optimized for higher speeds. The reduced number of computations in multiplication due to adjusting using concatenation operation and one carry save adder only, the designed multiplier offers significant improvement in speed. The designed modules are described in Verilog HDL. Logic synthesis and simulation are performed using the Xilinx Project Navigator. Finally the designed modules are implemented using Xilinx FPGA Spartan-3E family and device '*XC3S500efg320*' with speed grade of '-5'.

The fig. 6 shows simulation results for 8-bit multiplication of two numbers.

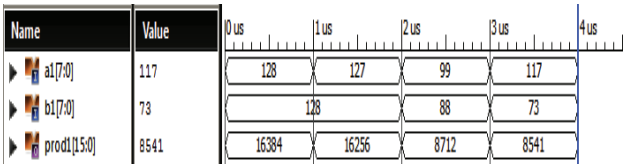

Fig. 6 8 x 8 Vedic Multiplier

The fig. 7 shows simulation results for 16-bit multiplication of two numbers.

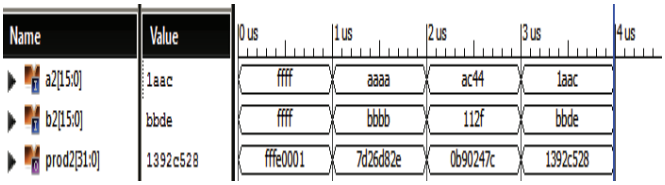

Fig. 7 16 x 16 Vedic Multiplier

The fig. 8 shows simulation results for 32-bit multiplication of two numbers.

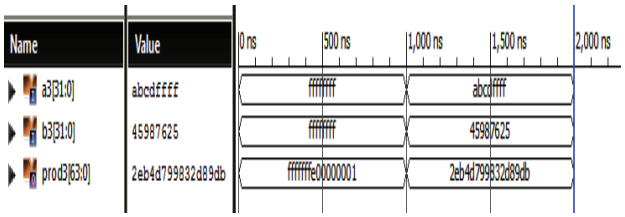

Fig. 8: 32 x 32 Vedic Multiplier

The fig. 9 shows simulation results for 8-bit squaring of two numbers.

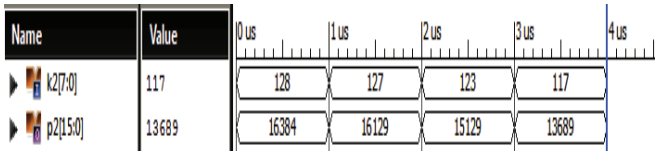

Fig. 9 8-bit Squaring module

The fig. 10 shows simulation results for 16-bit squaring of two numbers.

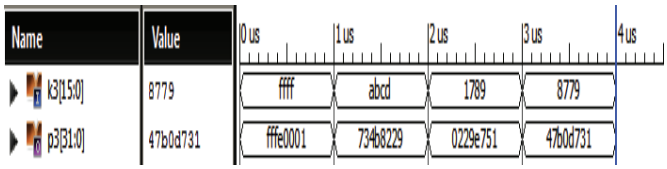

Fig. 10 16-bit Squaring module

The fig. 11 shows simulation results for 32-bit squaring of two numbers.

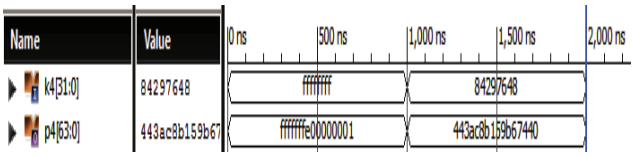

Fig. 11 32-bit Squaring module

The results for optimized multiplier module are compared with *G.Ganesh kumar et al. [6]*. The results for 32-bit multiplier are also compared with *Ravindra Patil et al. [14]*. The table I shows comparison of propagation delayfor multiplier modules of 8-bit,16-bit and 32-bit. The modules are implemented using Xilinx FPGA Spartan-3E family and device '*XC3S500efg320'* with speed grade of '-5'. The comparison results shows improvement of 28.72% for 32-bit multiplier modules.

Table I. Comparison of propagation delay (ns) results for multiplier modules

Bit Size	Propagation delay (ns)	
	[6]	This Work
8-bit	15.418	13.433
16-bit	22.604	17.617
32-bit	31.526	22.469

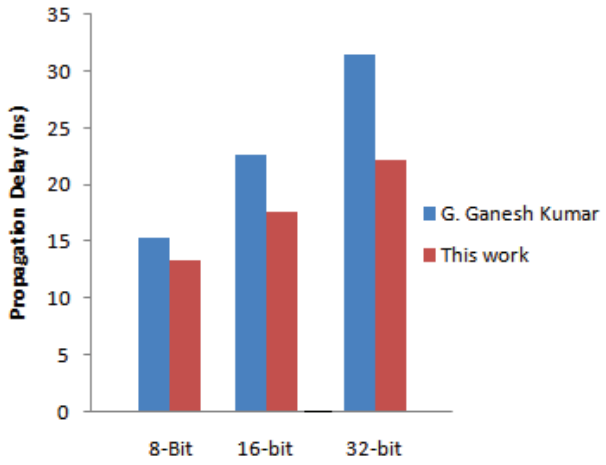

Fig. 12 Comparison of Propagation Delay (ns) for multiplier modules

The Table II shows comparison of propagation delay results for 32-bit multiplier module with *Ravindra Patil et al [14]*. The modules are implemented using Xilinx FPGA Spartan-3E family and device '*XC3S500epq280'* with speed grade of '-4'. The comparison results shows improvement of 38.59% for 32-bit squaring modules.

Table II. Comparison of propagation delay (ns) results for 32-bit multiplier module

Bit Size	Propagation delay (ns)	
	[14]	This Work
32-bit	41.562	25.520

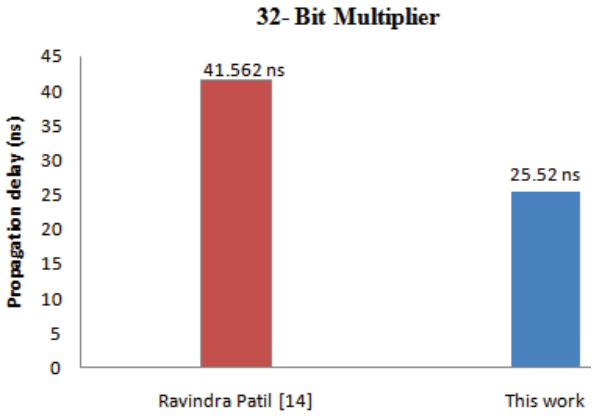

Fig. 13 Comparison of Propagation Delay (ns) for 32-multiplier modules

The table III shows comparison of propagation delay for squaring modules of 8-bit,16-bit and 32-bit. The modules are implemented using Xilinx FPGA Virtex-4 family and device '*vlx15sf363'* with speed grade of '-12'.

The results for optimized squaring module are compared with *Kabiraj Sethi et al. [7]*. The comparison results shows an improvement of propagation delay by 18.52%.

Table III. Comparison of propagation delay (ns) results for square modules

Bit Size	Propagation delay (ns)	
	[7]	This Work
8-bit	12.781	8.377
16-bit	15.994	10.800
32-bit	18.272	14.888

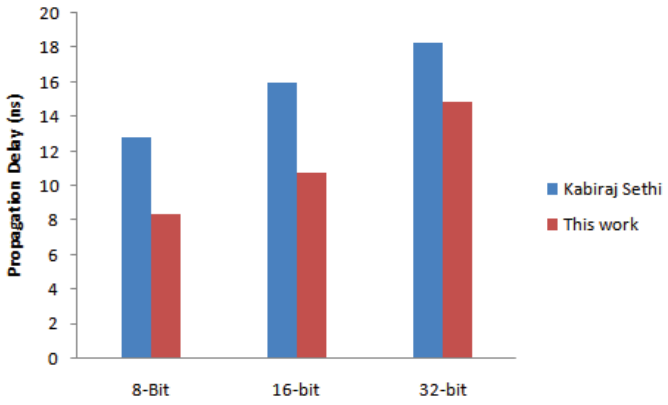

Fig. 14 Comparison of Propagation Delay (ns) for Squaring modules

CONCLUSION

The performance of the optimized Vedic multiplier and squaring architectures proved to be efficient in terms of speed. These architectures have regular structures. So, they can be realized easily on the silicon chip. It is also observed that as the number of bit size increases these architectures offer great improvement in delay. Future scope of the work is to increase the bits, analysis of power consumption and area.

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