About Voltage Total Harmonic Distortion for Single- and Three-Phase Multilevel Inverters

Alex Ruderman, *Member, IEEE*

***Abstract*—Many recent multilevel inverter papers end up with voltage total harmonic distortion (THD) values obtained from numerical voltage spectrum calculations (measurements). Motivated by IEEE Standard 519, a part of the multilevel research community uses a limited harmonic count to evaluate the multilevel voltage quality. First, this causes significant voltage THD underestimation, particularly for relatively high frequency PWM. Second, for a three-phase star-connected balanced load with an isolated neutral and phase symmetric modulation strategy, the calculated load line and phase voltage THD become different. However, simple considerations show that line and phase voltage THDs are essentially the same in this case. It may be difficult to judge about the multilevel voltage quality given a numerically calculated (measured) voltage THD value that may be subject to computation errors. Presented are simple smooth hyperbolic voltage THD upper and lower bound approximations for single- and three-phase inverters with nearest synchronous switching. They are valid for arbitrary modulation indices and uniformly distributed level counts and may practically serve as good reference values.**

***Index Terms*—DC–AC power conversion, multilevel inverters, pulsewidth-modulated power converters, voltage total harmonic distortion (THD).**

I. Introduction

MULTILEVEL inverters are being widely used for medium/high voltage and other applications [1]–[5]. Many recent multilevel inverter papers end up with voltage THD evaluation results that are typically based on voltage frequency spectrum numerical calculations/measurements (FFT).

A part of the multilevel research community uses a limited harmonic count (49 recommended by IEEE Standard 519 [6] or other like 101) to evaluate the multilevel voltage quality. First, this causes voltage THD underestimation that is especially significant for relatively high frequency PWM (an error may reach 100% and more). Second, for a practical case of a three-phase inverter with a star-connected balanced load with an isolated neutral, the THD of the line (line to line) voltage and that of the phase (line to neutral) one become different. However, simple time domain and symmetry-based considerations show that line and phase voltage THDs are the same in this case.

Some papers on cascade H-bridge three-phase converter with fundamental switching like [7] and [8] may seem misleading as they talk about different line and phase voltage THDs.

Manuscript received February 2, 2014; accepted June 7, 2014. Date of publication July 22, 2014; date of current version February 6, 2015.

The author is with the Electrical and Electronic Engineering Department, Nazarbayev University, Astana 010000, Kazakhstan (e-mail: alexander.ruderman@nu.edu.kz).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TIE.2014.2341557

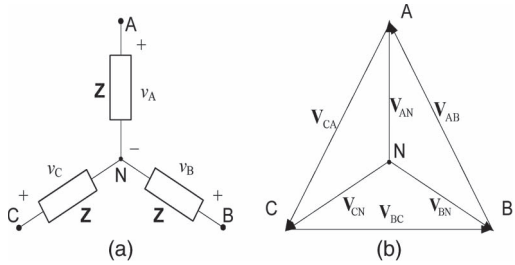

Fig. 1. Star-connected balanced three-phase load with isolated neutral. (a) Schematic. (b) Voltage-phasor diagram for a symmetrical load and supply.

Indeed, for the inverter side, phase (phase to inverter neutral) and line voltage THDs are different. However, for a star-connected balanced load with an isolated neutral, line and phase (phase to load neutral) voltage THDs have to be the same which is demonstrated hereinafter.

The theoretical upper bound that is achieved for an infinitely high switching frequency is practically quite accurate for the ratios of switching and fundamental frequencies that are larger than 25–30 and is valid for both single- and three-phase inverters [9]. The theoretical voltage quality lower bound is achieved for a minimum amount of synchronous switching that is once between any two adjacent voltage levels [10], [11].

Simple voltage THD upper and lower bound smooth approximations are suggested for the optimal voltage quality nearest synchronous switching for both single- and three-phase inverters.

For the cascaded H-bridge three-phase inverter, the relationship between the inverter and the load phase voltage quality is derived in the time domain. It clearly demonstrates that the load voltage quality is better and its improvement comes at the expense of load common-mode voltage deterioration.

II. Equivalence of Load Line and Phase Voltage THDs

For a three-phase star-connected balanced load with an isolated neutral (see Fig. 1), from the Kirchhoff voltage law, the relationship between instantaneous line and phase voltages is

$$v_{AB} = v_{AN} - v_{BN}, \quad v_{BC} = v_{BN} - v_{CN}$$
$$v_{CA} = v_{CN} - v_{AN}, \quad v_{AN} + v_{BN} + v_{CN} = 0. \tag{1}$$

As the same equations are valid for the line and phase voltage fundamental components, they also hold for the line and phase voltage ripples. The relationship between instantaneous line and phase voltage ripple squares from (1) becomes

$$v_{AB}^2 + v_{BC}^2 + v_{CA}^2 = 3\left(v_{AN}^2 + v_{BN}^2 + v_{CN}^2\right). \tag{2}$$

For a phase symmetrical modulation, after averaging on an ac fundamental period, the three line voltage mean ripple squares must be equal, and so do the three phase voltage ones. Then, (2) means the equivalence between the line and phase voltage THDs because the ratio between the line and phase voltage ripple rms values representing undesired harmonics content and fundamental line and phase voltage harmonic magnitudes is the same $-\sqrt{3}$.

This way, the elementary time domain consideration accounting for the load and phase modulation symmetry [9] makes the aforementioned proof almost trivial while the same result in the frequency domain is not so evident due to the fundamental difference between the line and phase voltage spectra.

III. Voltage THD Upper Bound

The single- and three-phase multilevel inverter voltage quality for relatively high switching frequencies was considered in [10]. The results are valid for optimal voltage quality nearest level/virtual space vector switching and present theoretical upper bound for synchronous switching. They are asymptotic in the sense that the ratio of the switching and fundamental frequencies is assumed infinitely large. Practically, the formulas become quite accurate for the said ratio above 25–30.

PWM voltage quality analysis is carried out in the time domain using the voltage ripple normalized mean square (NMS) criterion (the voltages are normalized with respect to a dc bus one). Voltage ripple NMS is obtained by two successive averaging operations—on a PWM period and on an ac fundamental one. The two averaging operations become independent due to the asymptotic assumption. Once the voltage ripple NMS is found, voltage THD can be calculated as

$$\mathrm{THD}_n(m),\% = \frac{\sqrt{2\mathrm{NMS}_n^{\mathrm{AC}}(m)}}{m}\cdot 100[\%] \tag{3}$$

where

n	(nonnegative) converter voltage level count (2 for a two-level inverter);
m	modulation index, $0 < m < 1$;
$\mathrm{NMS}_n^{\mathrm{AC}}(m)$	voltage ripple NMS expression.

For an arbitrary voltage level count, the voltage ripple NMS expression is piecewise analytical, employs only elementary functions, and is given by [9, eq. (10)]. Due to the asymptotic assumption (very high switching frequency), the voltage ripple NMS formula does not contain frequency dependences. Initially obtained for a single-phase (H-bridge) multilevel inverter, [9, eq. (10)] is valid for a three-phase inverter line voltage as well because the NMS criterion is invariant to voltage pulse redistribution within a PWM period (zero sequence insertion).

Some voltage THD graphs according to (3) are given in Fig. 2(a). Voltage THD versus m referred to $n+1$ levels and is obtained from that for n levels by scaling the x-axis $S = (n-1)/n$ times and adding the rightmost missing link for the m interval $(n-1)/n \le m < 1$.

Ignoring the NMS pulsation by using its average value [10]

$$\mathrm{NMS}_{n\_\mathrm{AV}}^{\mathrm{AC}} = \frac{1}{6(n-1)^2} \tag{4}$$

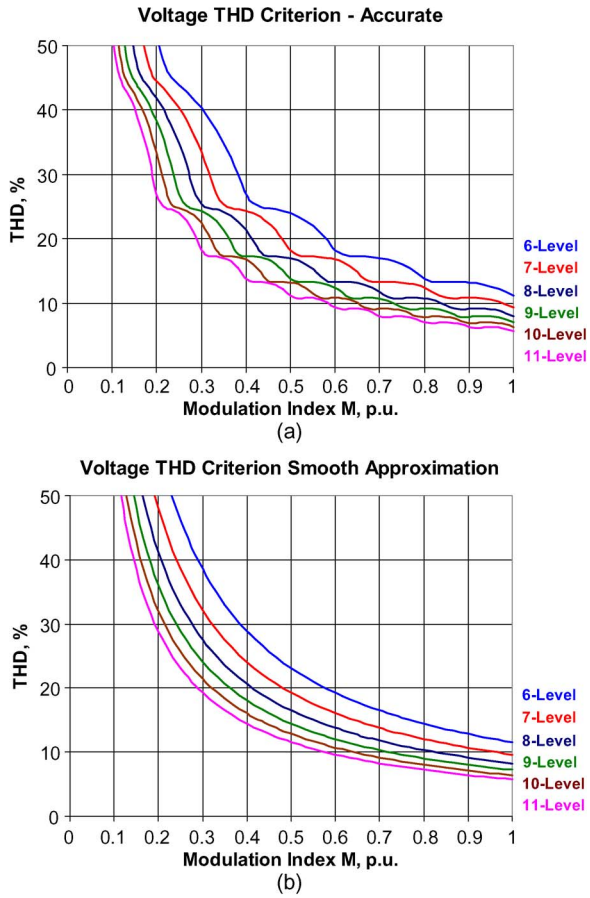

Fig. 2. Voltage THD upper bound for 6, 7, 8, 9, 10, and 11 levels: a—accurate according to (3) and (6); b—smooth approximation according to (5).

the voltage THD upper bound may be approximated in a ripple-free smooth manner as [10]

$$\mathrm{THD}_{\mathrm{SM}}^{\mathrm{UP}}(m,n),\% = \frac{1}{\sqrt{3}(n-1)m}\cdot 100\% = \frac{57.7}{(n-1)m},\%. \tag{5}$$

Formula (5) presents an approximate upper bound for both single- and three-phase inverters [see Fig. 2(b)] with the worst case accuracy being better than 5% for sufficiently large modulation indices.

IV. Voltage THD Lower Bound

The voltage quality lower bound is achieved for a minimal amount of nearest switching [10], [11], meaning switching once between any two adjacent voltage levels that is a staircase, or step, modulation (see Fig. 3).

Finding accurate voltage THD lower bound, in fact, means finding optimal switching angles that minimize quadratic approximation error (NMS). There are two major components of the associated optimization problem—problem formulation and solution method. The problem formulation in the frequency domain as a global optimization problem accounting for a limited harmonic count is a potential source of inaccuracy. In combination with metaheuristic optimization, it delivers sensitive unstable solutions that do not provide reliable predictable optimal switching angles and voltage THD [12].

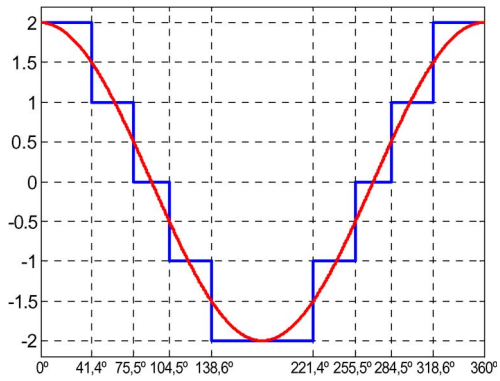

Fig. 3. Nearest switching strategy for a three-level single-phase inverter.

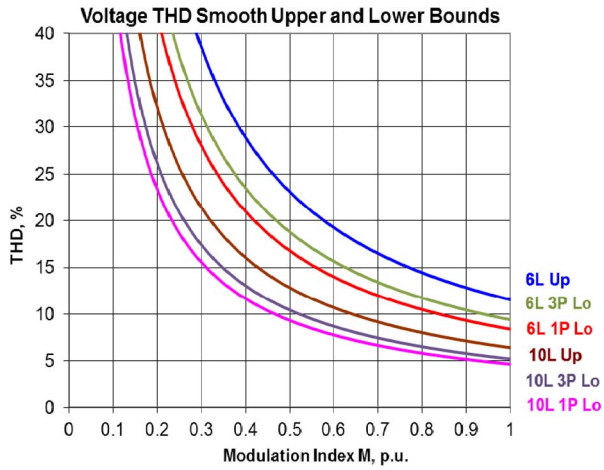

Fig. 4. Voltage THD smooth upper and lower bound comparison for single-and three-phase inverters for six and ten levels.

This way, the optimization problem must be formulated in the time domain as a constrained optimization one, thus taking into account all switching harmonics. The constraint is due to a fundamental voltage (modulation index) requirement. The accurate expression for a quadratic error to be minimized may be easily obtained by the squared voltage approximation error (see Fig. 3) analytical closed-form integration. A similar approach was applied to find the voltage THD lower bound local minima for different converter level counts $(L = 2, \ldots, 8)$ in [13] and [14], and the results obtained in both papers are identical.

Using the IEEE Standard 519 recommended harmonic count of 49 causes single-phase voltage THD underestimation that is about 7% for a three-level inverter and progressively increases with the level count increase (e.g., about 16% for a six-level converter) [15].

The voltage THD lower bound is mostly of theoretical interest because, as the minimum is "flat," it is a kind of ill-conditioned optimization problem and many different switching angle combinations can deliver near-optimal voltage quality.

Similar to (4) and (5), using an optimal NMS average value that is a numerically obtained NMS constant component for $0 < m < 1$, the voltage THD lower bound for single-phase inverters may be approximated in a smooth ripple-free manner as [10], [11]

$$\mathrm{THD}_{\mathrm{SM}}^{1,\mathrm{LOW}}(m,n),\% = \frac{42}{(n-1)m},\%. \tag{6}$$

Formula (6) ignores, as (5), THD pulsation and accurately renders the average trend with the worst case voltage THD error being of the order of 10% (of THD) for sufficiently large modulation indices. The maxima and minima of the voltage THD lower bound may be addressed separately if required.

Most of the aforementioned considerations for a single-phase inverter voltage THD lower bound are applicable to a three-phase inverter one. However, for a three-phase inverter, the voltage THD lower bound is larger due to interphase dependences because the switching angles cannot be selected independently and must fulfill additional constraints that arise from the quarter-wave symmetry and nearest switching requirements.

Using symmetry considerations, by time averaging, it can be shown that, for a three-phase cascade H-bridge inverter with a balanced three-phase load with an isolated neutral

$$\mathrm{NMS}_{\mathrm{Pn}} = \mathrm{NMS}_{\mathrm{PN}} - \mathrm{NMS}_{\mathrm{nN}} \tag{7}$$

where ripple voltage NMS terms refer to load phase-to-neutral, inverter phase-to-neutral, and load neutral-to-inverter neutral (common mode) voltages.

The major learnings from (7) are as follows.

1) Load phase voltage THD (ripple voltage NMS) is less than the inverter phase voltage one.
2) The optimal load voltage quality—minimal load phase voltage THD (ripple voltage NMS)—is achieved at the expense of common-mode voltage THD (NMS) increase.

For a three-phase inverter, the voltage THD lower bound smooth approximation becomes [11]

$$\mathrm{THD}_{\mathrm{SM}}^{3,\mathrm{LOW}}(m,n),\% = \frac{47}{(n-1)m},\% \tag{8}$$

that is 12% larger than that for a single-phase one (6).

Three-phase cascade H-bridge inverter load voltage THD bounds may be estimated based on line voltage waveform that has a nonnegative level count equal to $n = 2N$ (N—a number of cascaded two-level H-bridges in a single phase).

The voltage THD upper (5) and lower bound (6) and (8) smooth approximation comparison for six and ten converter levels is presented in Fig. 4.

V. Conclusion

It is shown that, for a three-phase star-connected balanced load with isolated neutral and phase symmetrical modulation, the line and phase voltage THDs are basically the same, independent of the multilevel inverter type employed.

As the major multilevel voltage quality improvement comes from increased level count, selected harmonics elimination and similar techniques do not make much practical sense for a relatively high level count as long as there are no specific voltage spectrum requirements.

Suggested simple hyperbolic voltage THD upper and lower bound approximations for single- and three-phase inverters are

valid for arbitrary modulation indices and equidistant level counts with a practical accuracy of 5%–10% of voltage THD and may serve as reliable initial reference values for practical measurements and calculations, often making numerical voltage THD calculations unnecessary.

REFERENCES

[1] J. Rodriguez, S. Bernet, B. Wu, J. O. Pontt, and S. Kouro, "Multilevel voltage-source-converter topologies for industrial medium-voltage drives," *IEEE Trans. Ind. Electron.*, vol. 54, no. 6, pp. 2930–2945, Dec. 2007.

[2] G. Buticchi, D. Barater, E. Lorenzani, C. Concari, and G. Franceschini, "A nine-level grid-connected converter topology for single-phase transformerless PV systems," *IEEE Trans. Ind. Electron.*, vol. 61, no. 8, pp. 3951–3960, Aug. 2014.

[3] L. Tarisciotti, P. Zanchetta, A. Watson, S. Bifaretti, and J. C. Clare, "Modulated model predictive control for a seven-level cascaded H-bridge back-to-back converter," *IEEE Trans. Ind. Electron.*, vol. 61, no. 8, pp. 3951–3960, Aug. 2014.

[4] C. Buccella, C. Cecati, M. G. Cimoroni, and K. Razi, "Analytical method for pattern generation in five-level cascaded H-bridge inverter using selective harmonic elimination," *IEEE Trans. Ind. Electron.*, vol. 61, no. 11, pp. 5811–5819, Nov. 2014.

[5] A. Mora, P. Lezana, and J. Juliet, "Control scheme for an induction motor fed by a cascade multicell converter under internal fault," *IEEE Trans. Ind. Electron.*, vol. 61, no. 11, pp. 5948–5955, Nov. 2014.

[6] *IEEE Recommended Practices and Requirements for Harmonic Control in Electrical Power Systems*, IEEE Std. 519-1992, 1993.

[7] N. Farokhnia, H. Vadizadeh, S. H. Fathi, and F. Anvariasl, "Calculating the formula of line voltage THD in multilevel inverter with unequal dc sources," *IEEE Trans. Ind. Electron.*, vol. 58, no. 8, pp. 3359–3372, Aug. 2011.

[8] N. Yousefpoor, S. H. Fathi, N. Farokhnia, and H. A. Abyaneh, "THD minimization applied directly on the line-to-line voltage of multilevel inverters," *IEEE Trans. Ind. Electron.*, vol. 59, no. 1, pp. 373–380, Jan. 2012.

[9] A. Ruderman, B. Reznikov, and S. Busquets-Monge, "Asymptotic time domain evaluation of a multilevel multiphase PWM converter voltage quality," *IEEE Trans. Ind. Electron.*, vol. 60, no. 5, pp. 1999–2009, May 2013.

[10] A. Ruderman, G. Mehlmann, and B. Reznikov, "PWM voltage quality bounds of a single-phase multilevel inverter," in *Proc. Int. Conf. OPTIM*, May 2012, pp. 58–68.

[11] G. Mehlmann, A. Ruderman, and G. Herold, "Voltage quality bounds of multilevel inverters," in *Proc. Int. ENERGYCON*, Sep. 2012, pp. 90–97.

[12] V. Roberge, M. Tarbouchi, and F. Okou, "Strategies to accelerate harmonic minimization in multilevel inverters using a parallel genetic algorithm on graphical processing unit," *IEEE Trans. Power Electron.*, vol. 29, no. 10, pp. 5087–5090, Oct. 2013.

[13] C. A. L. Espinosa, I. Portocarrero, and M. Izquierdo, "Minimization of THD and angles calculation for multilevel inverters," *Int. J. Eng. Technol. IJET-IJENS*, vol. 12, no. 5, pp. 83–86, Oct. 2012.

[14] F. L. Luo, "Investigating of best switching angles to obtain lowest THD for multilevel dc/ac inverters," in *Proc. 8th IEEE ICIEA*, Jun. 2013, pp. 1814–1818.

[15] B. Diong, "THD-optimal staircase modulation of single-phase multilevel inverters," in *Proc. IEEE Region 5 Conf.*, Apr. 2006, vol. 12, pp. 275–279.

Alex Ruderman (M'07) received the M.Sc. (with honors) degree from Leningrad Electrical Engineering Institute, Leningrad, Russia, in 1980 and the Ph.D. degree from Leningrad Polytechnic Institute, Leningrad, in 1987.

In 1995, he worked as a Research Scientist for the Intel Microprocessor Development Center, Haifa, Israel. In 2006, he joined Elmo Motion Control, Petach Tikva, Israel, as a Chief Scientist. He is currently an Associate Professor with the Electrical and Electronic Engineering Department, School of Engineering, Nazarbayev University, Astana, Kazakhstan.

Dr. Ruderman is a regular reviewer for the IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS and IEEE TRANSACTIONS ON POWER ELECTRONICS and an advisory/steering/scientific committee member for several international power electronics conferences. He is a member of the IEEE Power Electronics Technical Committee and an Associate Editor for *IET Power Electronics*.