An Enhanced Architecture for High Performance BIST TPG

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Abstract*—This paper proposes a methodology to generate the multiple test patterns varying in single bit position for built-in-self-test (BIST). The traditional patterns which were generated using Linear feedback shift registers lack correlation between consecutive test vectors. So, in order to improve correlation between the subsequent test vectors, the patterns were produced using Gray counter and Decoder. The Area optimization is achieved by reducing the total number of gate count to implement the design. In order to optimize the power, the number of toggles between the subsequent test vectors is curtailed. The generated test patterns have an advantage of minimum transition sequence. Simulation results on multiplier circuit shows a reduction of 54% in area overhead and 12% in power overhead compared to pattern generation using Reconfigurable Johnson counter and LFSR. 100% fault coverage is achieved while generating patterns using gray counter, decoder and accumulator architecture. Time coverage is same as time required for generating patterns using existing methodology.The methodology for producing the test vectors for BIST is coded using VHDL and simulations were performed with ModelSim 10.0b. The Area utilization and the power report were obtained with the help of Xilinx ISE 9.1 software.

***Index Terms*—Built-in-self-test (BIST), Test Pattern Generator (TPG), Multiple Single Input Change Vector (MSIC), Linear feedback shift registers (LFSR).**

I. INTRODUCTION

Testing plays a crucial role in any kind of production. The occurrence of imperfection in VLSI circuits results in testing every chip. The possibility of defect might be caused due to various constrains such as malfunctioning of equipments, design errors and material defect. Testing can be performed externally or internally. External testing is performed using automatic test equipment (ATE). The test vectors are generated using ATE and are applied to circuit under test (CUT). The results are analyzed using CAD tools. The drawback of performing testing using ATE is longer time required for testing and high cost of the equipment. Hence there is a shift from external testing to internal testing. Internal testing is performed with the help of built in self test (BIST). BIST reduces difficulty and complexity in testing the circuits. The test vectors generated are applied to the digital circuit and the circuit response obtained is compared with the true response to determine the fault. For the purpose of pattern generation exhaustive testing or Pseudo exhaustive testing or Pseudorandom testing can be performed. Exhaustive testing applies all possible input combination to the digital circuit. The advantage of generating test patterns using exhaustive testing is 100% fault coverage. But the drawback is the increased test time. In Pseudo exhaustive testing the circuits are partitioned into small slices and individual slices are tested using exhaustive testing. In Pseudorandom testing the patterns were generated in random fashion. The produced patterns may or may not be repeatable. The Pseudorandom patterns are generated to reduce the test length thereby reducing the time for testing.

In traditional techniques the testing vectors were produced using linear feedback shift register [1]. The limitation of generating test vectors is enormous switching operation between the successive test vectors. This frequent change over increases the power requirement. A survey has been performed by P.Girard in [2], on various external testing and internal testing methodologies. A.Abu-Issa and S. Quigley in [3], proposed the architecture to shrink the power dissipation by the process of interchanging the bits to LFSR. The scan chains are ordered initially. The test vectors were utilized by the scan chains and then the reordering process is carried out to improve the correlation among the test vectors. P.Girard et.al in [4], used simulated annealing algorithm to curtail the energy.

S.Wang and S.Gupta in [5], used two LFSR operating at varying speed to shrink the unwanted transitions. F.Corno et.al developed a test pattern generator for shrinking the power necessary in combinational circuits [6]. P.Girard et.al in [7], adjusted the clock pulse for decreasing the power. Instead of applying single clock pulse two separate clock pulses were produced. D. Gizopoulos et.al in [8] proposed a methodology to produce deterministic patterns for testing data paths. In [9]

Bonhomme et.al proposed a methodology to gate the clock producing the unwanted transition. The scan cells were split into odd and even scan cells. The odd scan cells were controlled with the help of first clock pulse and even scan cells were controlled with the help of second clock pulse. The drawback of this technique is generation of two distinct clocks. In [11], Laoudias.C produced test vectors with the help of ring generator. The outcomes are evaluated against the predicted values. Bhunia et al. placed extra transistor in the path to ground. The partial gating system has been preferred to diminish the power requirement [12].

The rest of the paper is organized as follows. In Section II, the Existing Methodology is presented. In Section III, the Proposed Methodology is presented. In Section IV, the Simulation results and analysis is presented. Conclusion is given in Section V.

II. EXISTING METHODOLOGY

The existing method involves producing testing vectors for built in self test [13]. The vectors were produced by performing xor operation between seed vector and reconfigurable Johnson counter [14]. The test set generated was applied to the multiplier circuit. The faults were detected by comparing the response of the circuit with the expected response.

A. Pattern Generation

The existing technique generates the test pattern using Johnson counter and the seed vector. Reconfigurable Johnson counter generates the Johnson vector and Linear Feedback Shift Registers generates seed vector. Test patterns were generated by performing Exclusive-or operations between Johnson counter and seed vector [14]. The vectors obtained were utilized by the scan chain.

The pattern generation method for BIST shown in Fig.1 involves performing xor operation between the seed vector and reconfigurable Johnson counter. The Johnson counter generates Johnson vector and the seed block generates the seed vector. The results obtained were loaded into the scan chain. The vectors are circularly shifted continuously and xor operation is performed with the seed vector. The procedure is repeated until all the scan cells are loaded. The eight bit patterns generated were tested on 4*4 Multiplier circuits.

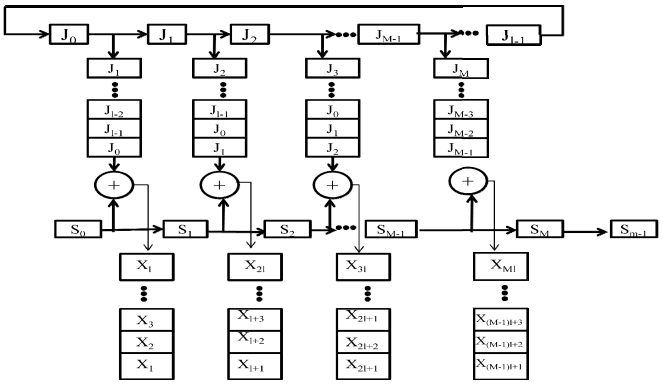

Fig. 1. Test vector generation[14]

B. Generation of Johnson vector

The Johnson vectors were produced by utilizing reconfigurable Johnson Counter. Reconfigurable Johnson counter is constructed with the help of an AND gate, Multiplexer and eight Delay flip flops are connected together to store the bits. Johnson vector were made to operate in Initialization mode, Circular shift mode and Normal mode. To initialize the flip flops the select input of the multiplexer is assigned with the value 1 and one of the inputs to the AND gate is assigned with the value 0. The clock signal is applied to initialize the registers. Fig.2. indicates the initialization operation of the Reconfigurable Johnson counter. The circular shift mode performs shifting operation and the output Q_8 of D_8 register is fedback. To perform circular shift operation the select input of the multiplexer is chosen to be 1 and input to the AND gate Init is assigned with the value 1. The clock input is clocked to operate Johnson counter in circular mode. The circular shift operation of Johnson counter is shown in Fig.3. While operating in normal mode the inverted bit corresponding to last flip flop is fedback as shown in Fig.4.

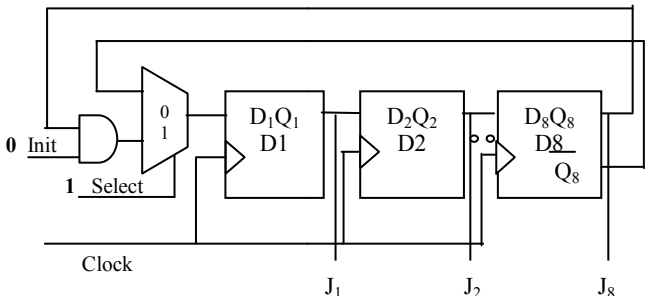

Fig.2. Initialization operation [14]

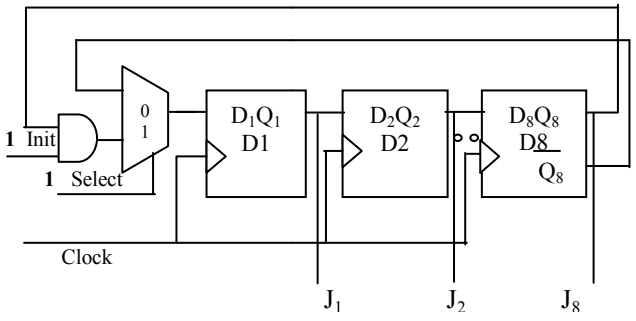

Fig.3. Circular shift operation [14]

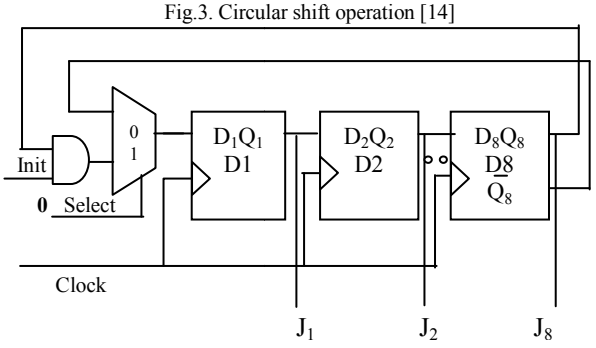

Fig.4. Normal mode [14]

C. TPG using test per clock

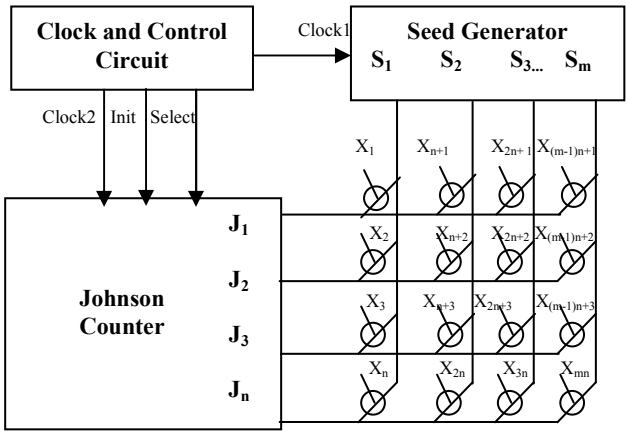

Fig. 5. Pattern generation [14]

The xor gate receives input from Johnson counter and seed generator. The clock signal clock1 and clock2 were generated using clock and control circuit. The clock signal clock1 is applied to seed generator block to produce seed vector. The clock signal clock2 is applied to Johnson counter block to produce Johnson vector.

The following procedure is adopted to generate the patterns

1) The clock signal Clock1 is clocked to produce the seed.
2) The clock signal Clock2 is clocked to produce Johnson vector.
3) Generate 2*l* Johnson vectors by repeating step 2.
4) Steps 1-3 were repeated until the specified test length is achieved.

III. PROPOSED METHODOLOGY

The demand for the portable devices is increasing tremendously. So Area and Power optimization are essential to satisfy the demands of the consumer. The patterns generated using Existing methodology finds complexity in Area and Power. For the purpose of optimization the patterns were generated using Gray code counter. The purpose of choosing gray code counter is to reduce the power requirements. The gray code counters prevent the unwanted signal transition at the input. The input bits vary in single bit position. For every rising edge of the clock four bit gray code results were applied to 3 to 8 Decoder circuit. The results of decoder circuit were applied to the adder circuit through Register B. The set reset flip flop is used as Register A to store the computed result. The patterns were obtained through register A. The patterns produced were tested on Multiplier circuit. The response obtained is compared with the forecasted result to verify the exact functioning of the circuit.

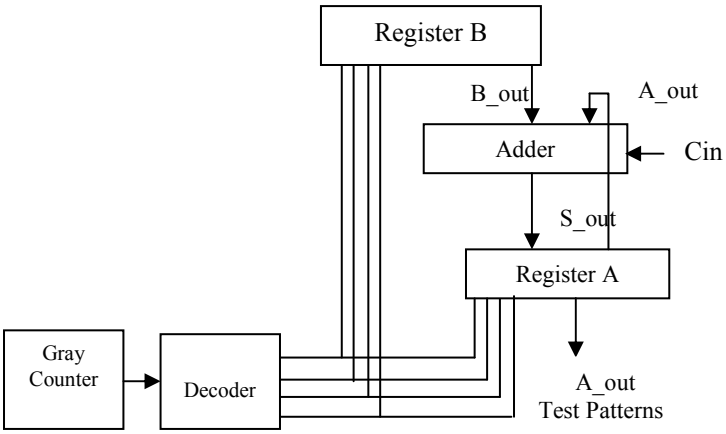

Fig. 6. TPG using gray counter

The proposed architecture has an advantage of occupying lesser gate count thereby minimizing the complexity of the circuit. The patterns generated vary in single bit position that reduces the unwanted transition thereby reducing the power requirements.

IV. SIMULATION RESULS AND ANALYSIS

The various design of the test pattern generation for BIST is implemented using front end ModelSim 10.0b software and Xilinx ISE 9.1 software. The design is coded in VHDL and simulations were performed using ModelSim 10.0b software. The test patterns generated were tested on 4*4 Multiplier circuit. The analysis of area and power are performed using Xilinx ISE 9.1 software.

The simulation result for implementing pattern generation using reconfigurable Johnson counter and seed vector is determined using ModelSim 10.0b software. The clock signal clk2 is clocked to generate the Johnson vector. The input to the seed vector is '01101'. The patterns generated were shown in the Fig.7.

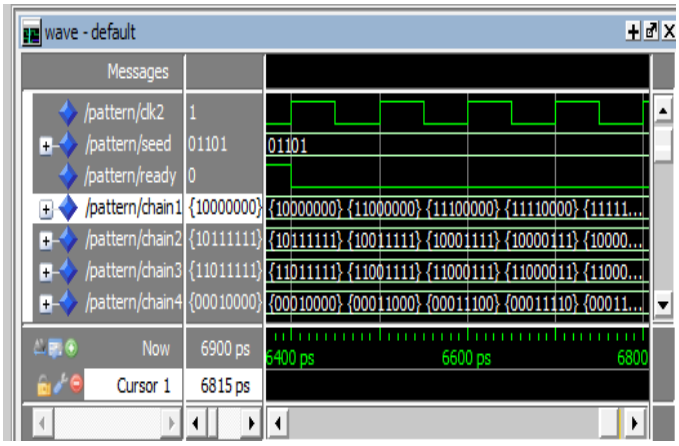

Fig. 7. TPG using Reconfigurable Johnson counter and LFSR

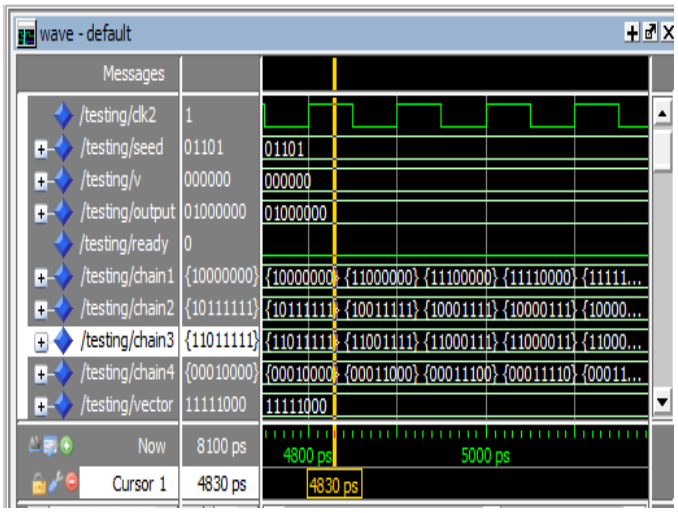

Fig. 8. Testing of Multiplier using Reconfigurable Johnson counter and LFSR

The faults were injected into the multiplier circuit. Fig.8. shows testing of multiplier circuit by considering stuck at 0 fault at the first input bit. The clock signal clk2 is clocked to generate Johnson vector. The input to the seed vector is '01101'. The input v is fed as "000000" indicating stuck at 0 fault at the first input bit. The expected result is compared with the predicted result to verify whether the fault is identified by the test pattern.

Since the Existing methodology had various demerits in area and power, to overcome these limitations the architecture is modified by producing the patterns using gray code counter. The simulation result for generating patterns using Gray counter using ModelSim 10.0b software is shown in Fig.9. The clock pulse is applied to the input clock. The input b_in to the Register B is "00000000". For every clock pulse the pattern_out is the required test pattern.

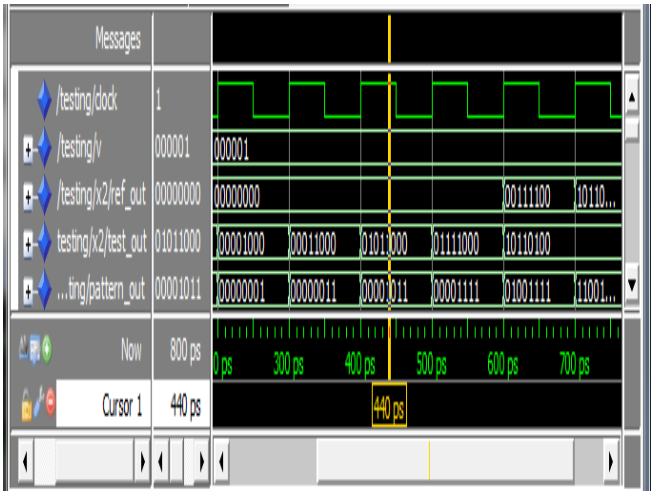

Fig.9.TPG using gray counter, decoder and accumulator

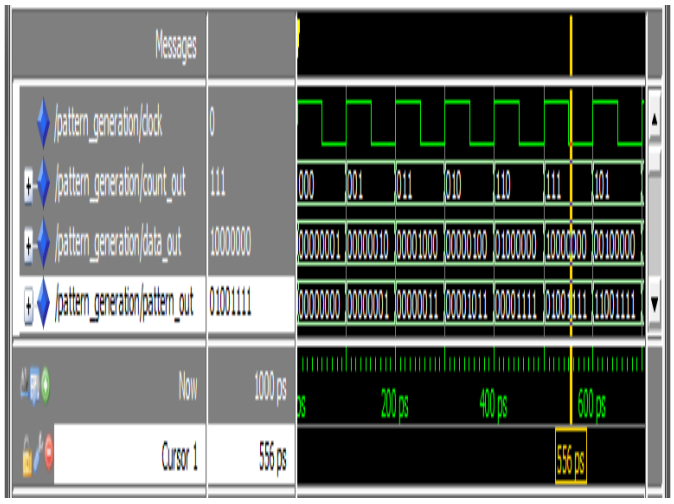

Fig.10. Testing of Multiplier using gray counter, decoder and accumulator

The faults were injected into the multiplier circuit. Fig.10. shows testing of multiplier circuit by considering stuck at 1 fault at the first input bit. The clock signal clock is clocked to produce the gray code output which in turn fed to the decoder circuit. The input v is fed as "000001" indicating stuck at 1 fault at the first input bit. The expected result is computed by the signal ref_out. The predicted result is computed by the signal test_out. The expected result is compared with the predicted result to verify whether the fault is identified by the test pattern.

The Area report for generating patterns is determined using Xilinx ISE 9.1 is as shown in Fig.11. The Power report for generating patterns is determined using Xilinx ISE 9.1 is as shown in Fig.12. The test length report is as shown in the Fig.13. For implementing the testing on multiplier circuit using Reconfigurable Johnson counter and seed vector, 312 gates were required. The total power estimation is 41.79 mW. The processing time delay is 23.511ns. 100% fault coverage is achieved while generating patterns using Reconfigurable Johnson counter and seed vector. The total number of patterns required to cover all possible stuck-at-faults is 12. For implementing the testing on multiplier circuit using gray counter, decoder and accumulator architecture 142 gates were required. The total power estimation is 36.75mW. The processing time delay is 23.511ns. 100% fault coverage is achieved while generating patterns using Reconfigurable Johnson counter and seed vector. The total number of patterns required to cover all possible stuck-at-faults is 14. The Analysis report of Area and Power for generating TPG using Reconfigurable Johnson counter and LFSR and gray counter, decoder and accumulator has been tabulated. The results shows that the patterns generated using Gray counter could be more efficient by utilizing less number of gates and reducing power requirement.

TABLE I ANALYSIS REPORT

	AREA (Gate Count)	POWER (mW)	TEST LENGTH
RECONFIGURABLE JOHNSON COUNTER AND LFSR	312	41.79	12
COUNTER, DECODER AND ACCUMULATOR	142	36.75	14

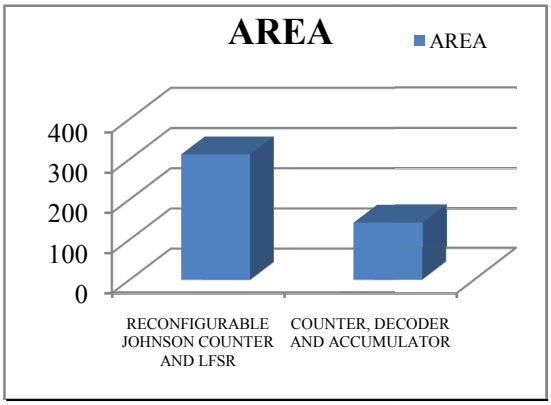

Fig.14. Area Report

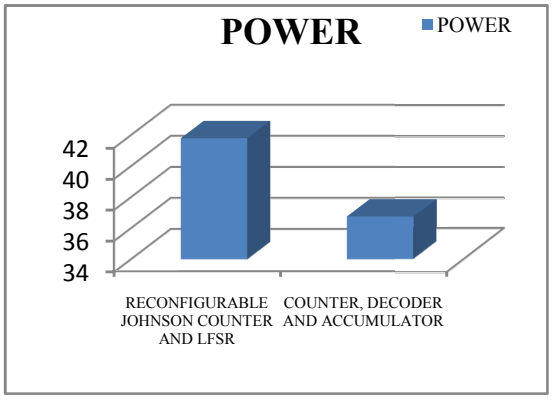

Fig. 12. Power Report

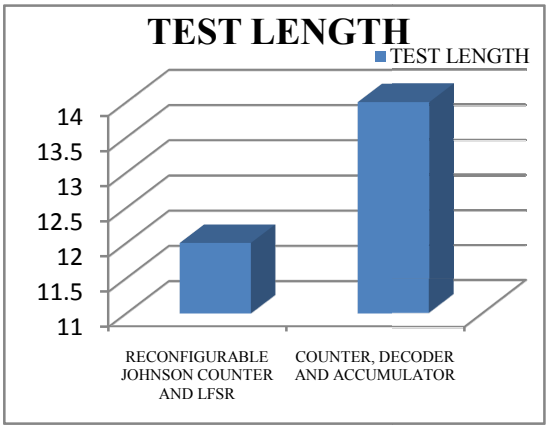

Fig. 13. Test Length Report

V. CONCLUSION

The architecture has been proposed to generate the test patterns for BIST. Power optimization and Area Optimization is achieved by generating patterns using Gray counter. The proposed architectures have the ability of detecting the faults occurring in a combinational circuit. The single input change patterns generated, improve the correlation between the successive test patterns thereby reducing power requirements. This technique to generate the multiple test patterns varying in single bit position for BIST schemes is coded using VHDL and simulated using ModelSim 10.0b. The gate count and power consumption of the test pattern generation were analyzed using Xilinx ISE 9.1 software. Simulation results show that the pattern generation using gray counter, decoder and accumulator reduces 54% of area overhead and 12% of power overhead compared to pattern generation using reconfigurable Johnson counter and LFSR. 100% fault coverage is achieved while generating patterns using Gray counter, decoder and accumulator architecture. Time coverage is same as that of existing methodology.

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