An Asymmetric Multilevel Inverter Using Reduced Switch Count Topology

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***Abstract*— A basic unit configuration which uses very less number of switches for obtaining an asymmetric multilevel inverter is proposed in this paper. Even and odd voltage levels at the output can be achieved by adding a conventional inverter bridge circuit to basic unit. Asymmetric configurations have different value of dc sources, so large number of levels will obtained at the output with reduced number of semiconductor devices, which make control easier with high power quality and lower harmonics. MATLAB Simulink model of a 11- level inverter with fundamental and high frequency control are performed and compared the results and harmonic spectra.**

Keywords—asymmetric cascaded multilevel inverter; harmonics; switching devices; low frequency control ; high frequency control; total harmonic distortion;

I. INTRODUCTION

There are tremendous categories of multilevel inverters such as diode clamped, capacitor clamped, cascaded, generalized, mixed level hybrid, asymmetric hybrid soft switched multilevel cells, etc. [1] They have evolved from the need of obtaining high quality, lower harmonics and switching losses and better electromagnetic interferences. Since the cascaded inverter does not contain any high rating capacitors and diodes, make the implementation and control of it easier and reduces over all installation space also [2]. Symmetric inverter with same amplitude of voltage source and asymmetric inverters with different amplitudes of dc sources are the two different configurations of this type. While using asymmetric configuration, output voltage with more steps will help to decrease the total harmonic distortion (THD) [3]. Several modulation and control strategies are available for multilevel inverters based on the type of inverter used and switching frequency at which the inverter works with, which will also help for reduction of THD. Space vector control and selective harmonic elimination are the type of low frequency control techniques while space vector pulse width modulation (PWM) and sine PWM included in high frequency switching technique.

This paper explains about an asymmetric cascaded multilevel inverter using reduced number of switches that are controlled by pulse width modulation. Simulink model and Fourier analysis on this circuit performed for verifying the results and evaluating the THD of current and voltage.

II. PROPOSED TOPOLOGY

A. Basic unit

The basic unit with reduced switch count topology of asymmetric cascaded inverter consists of five switching devices and three voltage sources as in fig.1. The switching of this structure is such that, the output voltage will have the values 0, (V_1+V_3), (V_1+V_2+V_3) when switches S_5, (S_1, S_3, S_4) and (S_1, S_2, S_3) are in on position respectively as given in the table 1.

An additional dc voltage source with magnitude same as that of first voltage source is added series to it through two unidirectional switches as shown in fig.2 for producing magnitude of this voltage level as the lowest output level.

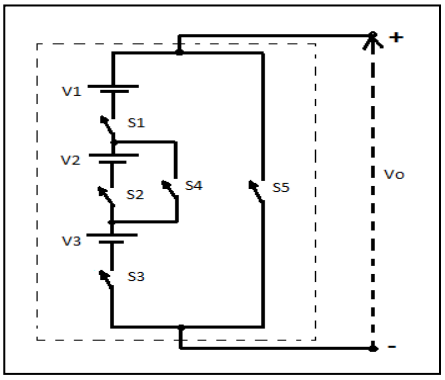

Fig. 1. Basic unit of asymmetric cascaded inverter

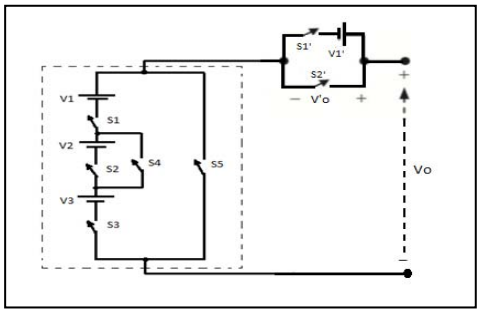

Fig. 2. Basic unit of asymmetric cascaded inverter with additional unit

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TABLE I. Switching States

State	Switching State					Vo
	S1	S2	S3	S4	S5	
1	Off	Off	Off	Off	On	0
2	On	Off	On	On	Off	V1+V3
3	On	On	On	Off	Off	V1+V2+V3

Make sure that the power devices (S_2, S_4), (S_1, S_3, S_4, S_5), (S_1, S_2, S_3, S_5) and (S_1', S_2') should not on simultaneously to avoid the short circuiting of DC sources. Any number of unit can be seriesly connected to produce high levels, since THD get reduced while level increases. Equation (1) is the total output voltage produced when $V_{O,1}(t)$, $V_{O,2}(t)$,….etc $V_{O,n}(t)$ are the voltages of first, second and up to nth unit connected in series and $V'_O(t)$ is the voltage of additional unit.

$$V_{O(t)} = V_{O,1}(t) + V_{O,2}(t) + \cdots + V_{O,n}(t) + V'_O(t) \quad (1)$$

A conventional inverter bridge circuit inserted to the combination of basic and additional unit to generate all the positive and negative levels since the combination only have positive levels at the out. Hence the total number of power devices and sources used by asymmetric inverter is given by the following equations in terms of number of series connected unit n.

$$N_{switch} = 5n + 6 \quad (2)$$

$$N_{source} = 3n + 1 \quad (3)$$

Comparing with other circuits this basic unit and its cascded inverters are more effective for high levels because they reduce amount of switches used when level increases. The maximum blocking voltage of semiconductor switches are the one of main parameters determining cost of system. Considering the fig.2, the blocking voltage calculated as

$$V_{block} = (v_{block} + v'_{block} + v_{block,\,H}) \quad (4)$$

Here v_{block}, v'_{block} and $v_{block,\,H}$ are the blocking voltages of basic unit, additional basic units and bridge circuit respectively.

B. Control and Modulation

Both high frequency and low frequency modulation methods can be applied for the circuit depending on their applications. The fundamental frequency modulation technique results low switching losses and switching stresses compared to another method, but in aspects of total harmonic distortion, the latter will give a more feasible output.

Sinusoidal pulse width modulation scheme is generally used for high frequency switching, which includes

(1) All the carriers are alternatively in phase opposition (APO) disposition.

(2) All the carriers above the zero reference are in phase and below are in phase opposition (PO) disposition.

(3) All the carriers are in phase (PH) disposition.

The PO disposition PWM method is more suitable for this asymmetric inverter.

Considering n number of series connected units, the magnitude of voltage source used and corresponding number of levels obtained by the asymmetric cascaded inverter calculated by the (5), (6), (7) respectively.

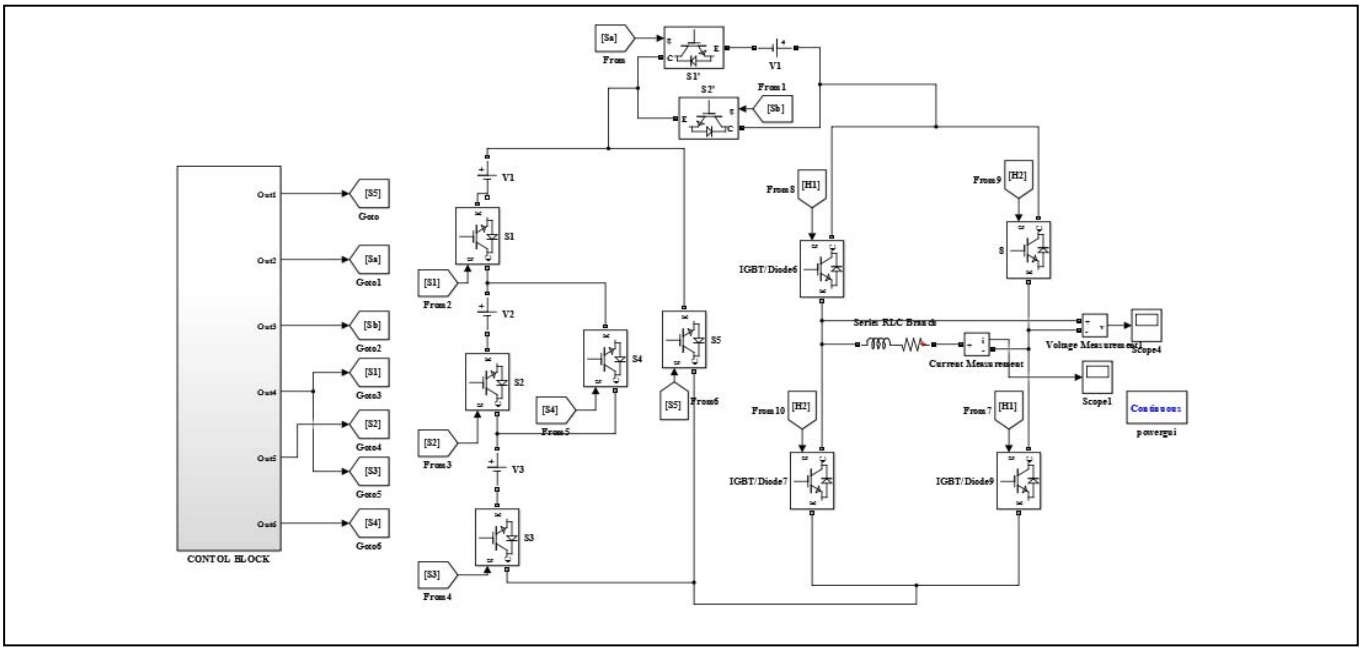

Fig. 3. Simulink model of asymmetric cascaded multilevel inverter

$$V_{j1} = 0.5 \quad (5)$$

$$V_{j2} = V_{j3} = 2^{j-1}V_{dc} \qquad \text{for } j=1, 2\ldots n \quad (6)$$

$$N_{level} = 2^{n+3} - 5 \quad (7)$$

Evaluating the above equations, the single unit capable of producing a 11 output levels.

III. Simulation And Results

The MATLAB Simulink model of asymmetric cascaded inverter is shown in fig.3, which includes basic unit, additional unit, inverter H- Bridge and control block diagram. The control of switches by using fundamental frequency and high frequency with PWM are performed and the outputs are verified.

A. Fundamental frequency switching

Output voltage and current waveforms generated by a single unit when controlled using a low frequency modulation method is shown in fig.4 and fig.5 respectively.

The load used for the circuit is resistance- inductor, so current correponds to the voltage will lag the voltage for some angle but the structure is more sinusoidal.

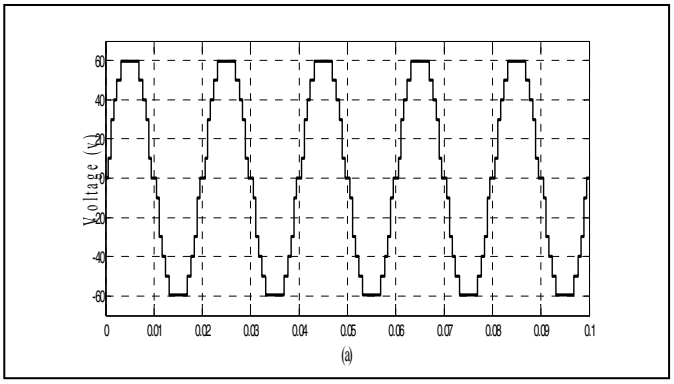

Fig. 4. Output voltage waveform of 11-level asymmetric cascaded multilevel inverter

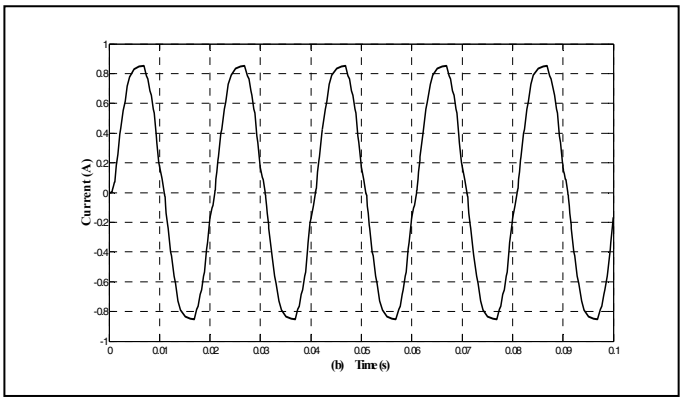

Fig. 5. Output current waveform of 11-level asymmetric cascaded multilevel inverter

B. High frequency switching

High frequency sine PWM control also verified for the circuit and the output voltages and currents corresponds to this is shown in fig.6 and fig.7 respectively.

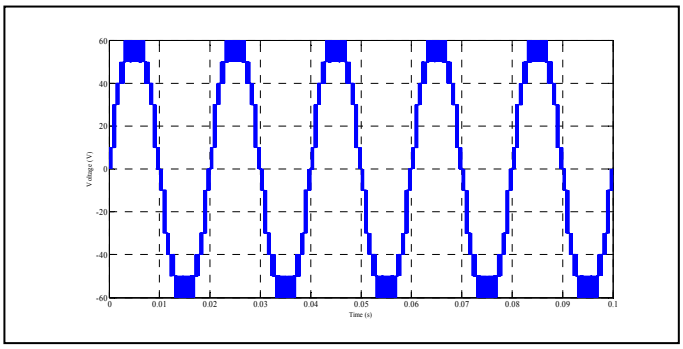

Fig. 6. Output voltage waveform of 11-level asymmetric cascaded multilevel inverter with PWM

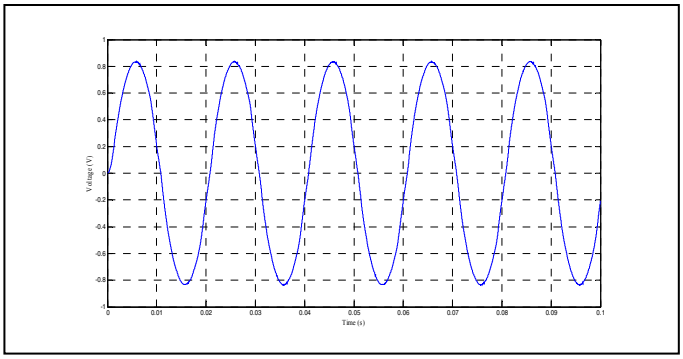

Fig. 7. Output current waveform of 11-level asymmetric cascaded multilevel inverter with PWM.

C. Fourier analysis

The harmonic spectrum of output voltage and current for both modulation techniques are also evaluated, it can be analysed that current harmonic of PWM controlled inverter is less compared with low frequency control.

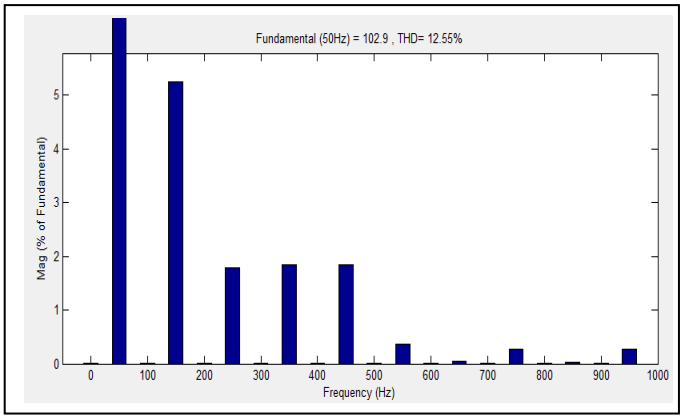

Fig. 8. Harmonic spectrum of voltage using fundumental frequency

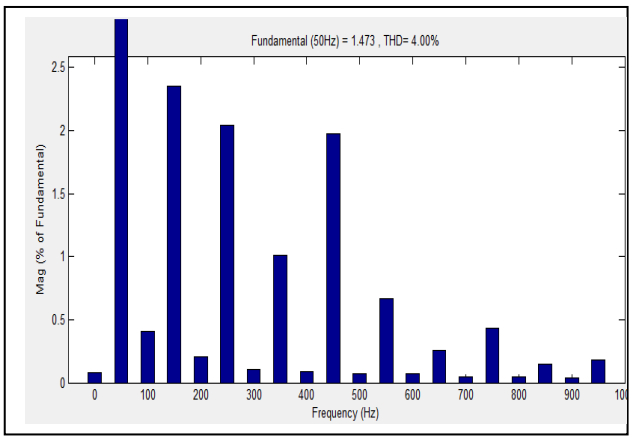

Fig. 9. Harmonic spectrum of current using fundumental frequency

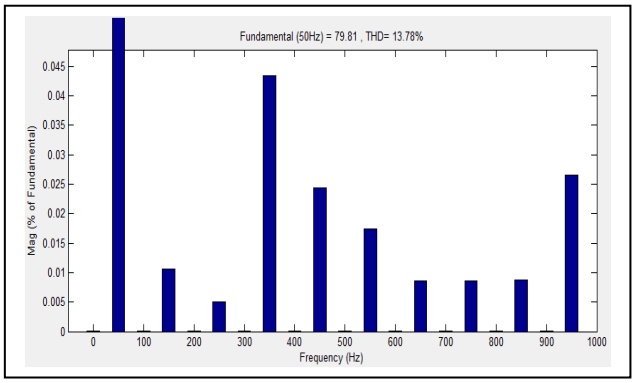

Fig. 10. Harmonic spectrum of voltage using PWM

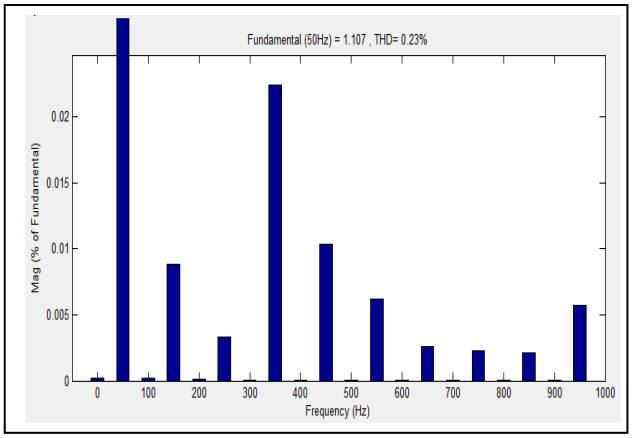

Fig. 11. Harmonic spectrum of current using PWM

The fundamental and higher order harmonics in the voltage and current for fundamental switching is 12.55% and 4% as shown in fig8 and fig.9 and for PWM switching, it is 13.7% and 0.23% as shown in fig.10 and fig.11. The total harmonic distortion will again reduce to a very small value for large number of levels and series connected units. The output can generate a 27-level output when two units connected in series.

IV. Conclusion

An asymmetric cascaded multilevel inverter configuration explained in this paper with a different basic unit, which includes reduced number switching devices for easier control less implementation cost and installation space. The levels are increased by series connection of individual units up to any number of levels. Modulation with low and high frequencies are also compared and the total harmonic distortion analysed through Fourier analysis. The Simulink model of single unit with H-Bridge is performed by MATLAB and the results are verified.

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